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Fisica delle Nanotecnologie – part 4

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Materiali, tecnologie e metodi per il data storage: problematiche di miniaturizzazione e nanotecnologie

17/11/2005 – 16.30-18 – room T1

Introduction to the topic

Data storage: key point in Information Technology, thus miniaturization to the nanoscale range is an obvious requirement

*In general, data storage implies the ability to convert electrical signals into a permanent or semi-permanent modification of a state, and to read such modification by electrical means: devices can be considered **passive** when retention is concerned but **active** during read or write operations*

The topics involves:

- **Fundamental mechanisms** for data storage (e.g., mechanical, electronics, magnetics, optical, ...);
- **Materials** where a state can be easily modified (either in a permanent, non-volatile or volatile mode) and modifications can be easily detected;
- *Techniques for writing/reading information*;
- *Technologies for material and device fabrication*;
- **Nanotechnology** for extreme miniaturization

Outlook

- A few words on Random Access Memories (DRAM) and on flash memories: materials issues in miniaturization

- Nanosized memories: proposals to use single electrons and quantum dots

- Materials for ferroelectric capacitors (inorganics and organics)

- Data storage with ferromagnetic materials:
  - giant magnetoresistance in nanostructured materials;
  - the superparamagnetic limit in the present mass-storage technology

- Optical storage:
  - read-only and write-only;
  - phase-changing materials for re-writable applications;
  - fundamental and technological limits in optical methods

- A few words on nanowriting on photoaddresable polymers (photopolymers) and on alternative nanotechnological approaches (e.g., millipede, optical near-field - *we will see more on that!*)

Overview of some methods and materials for data storage

Method	Mechanism	Examples	Problems/issues
electronic	Charge stored in a capacitor	DRAM, ROM, flash,...	Tunneling, single electron, Coulomb blockade,...
magnetic	Domain magnetization	Hard-disk	Mechanics, superparamagnetism
optical	Local change of optical properties	CD-ROM, CD-RW, DVD, ...	Mechanics, optical diffraction, optical near field

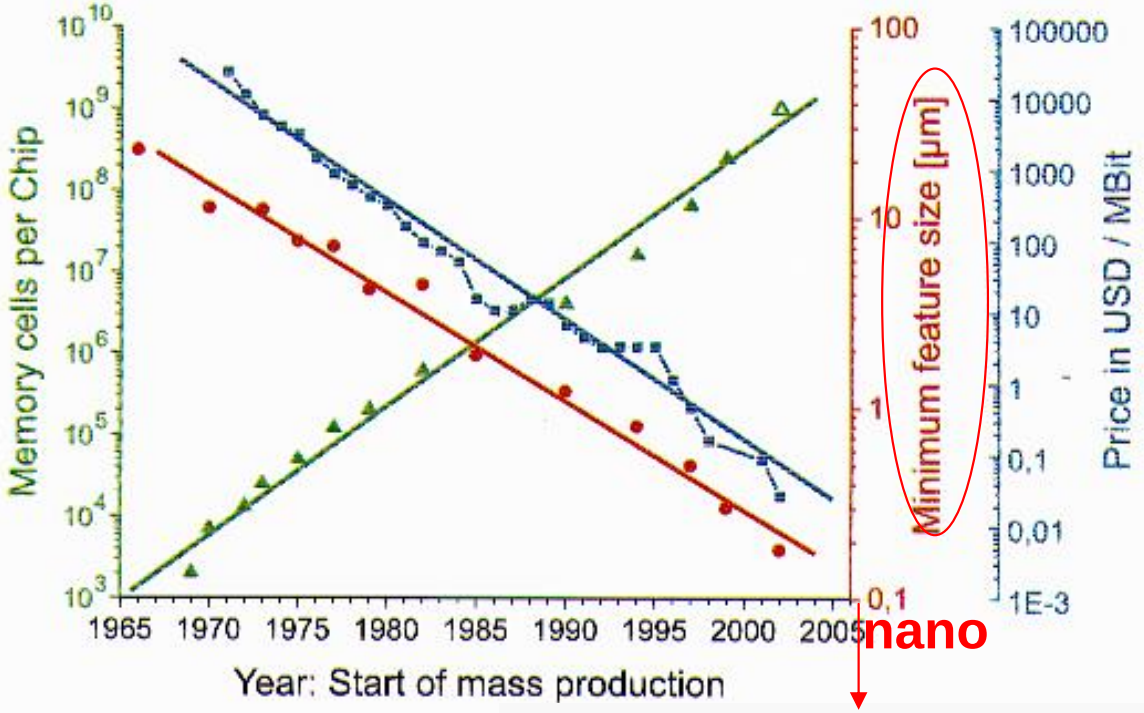
Huge expectations for further miniaturization

⇩

Nanotechnological problems/issues

Example: Random Access Memories (RAM)

Essential component of any IT system or device



Economy greatly relevant

ITRS Technology Nodes and Chip Capabilities[2]				
	2001	**2005**	**2010**	**2016**
DRAM Half-Pitch (nanometers)	130	80	45	22
DRAM Memory Size (mega or gigabits)	512M	2G	8G	64G
DRAM Cost/Bit (micro-cents)	7.7	1.9	0.34	0.042
Microprocessor Physical Gate Length (nanometers)	65	32	18	9
Microprocessor Speeds (MHz)	1,684	5,173	11,511	28,751

Basics of DRAM operation

2 Basic Operation of DRAM Cells

The 1T-1C DRAM cell has quite a simple structure (see Figure 2). The access transistor, Tr, acts as a switch and is addressed by the word line, WL, controlling the gate. The memory capacitor, C_S, represents the charge storage element for the information and is connected to the bit line, BL, via the transistor. When the switch is closed the information, the voltage levels $+V_{DD}/2$ or $-V_{DD}/2$ are applied to C_S via BL. The corresponding charge on C_S represents the binary information, "1" or "0". After this write pulse (e.g. for the 256 Mb generation this pulse is less than 10 ns at $V_{DD}/2 = 1.25$V) the capacitor is disconnected by opening the transistor switch.

The memory state is read by closing the switch and sensing the charge on the capacitor via the bit line, which is usually pre-charged to $V_{DD}/2$. The cell charge is redistributed between the cell capacitance, C_S, and the bit line capacitance, C_{BL}, leading to a voltage change in the bit line. This voltage change is detected by the sense amplifier in the bit line and amplified for the subsequent use of the read information as described in Sect. 3 of the Introduction to Part IV. As a read pulse destroys the charge state of the capacitor, it has to be followed by a re-write pulse to maintain the stored information. The plate line, PL, is kept at $V_{DD}/2$ in order to reduce the electric voltage stress on the capacitor dielectric, which is charged to $\pm V_{DD}/2$ instead of being discharged to 0 V and charged to full V_{DD}.

The DRAM is volatile, i.e. the information, the stored capacitor charge, is lost after the supply voltage is cut. In addition, the stored charge decreases with time because of leakage currents through both, the capacitor and the transistor. In order to guarantee a certain charge and, thus, a corresponding minimum voltage change in the BL detectable by the sense amplifier during the read operation, the charge of each memory capacitor has to be refreshed periodically. For the 256 Mb generation, the refresh time is about 64 ms [6]. In general, by selecting a WL all the select-transistors in this row are active so that all cells in this row (1024 or 2048, depending on organization) can be read simultaneously. As mentioned above, those cells are then refreshed by the necessary re-write. A special built-in counter takes care of the refresh for those rows which are not selected by the working program during the given refresh period.

DRAM = MOS-FET + capacitor

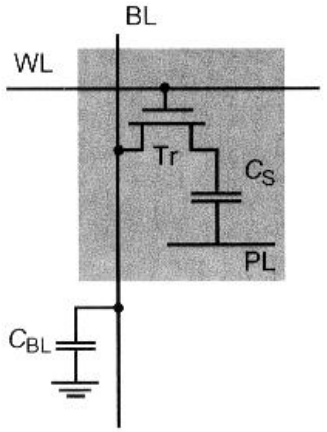


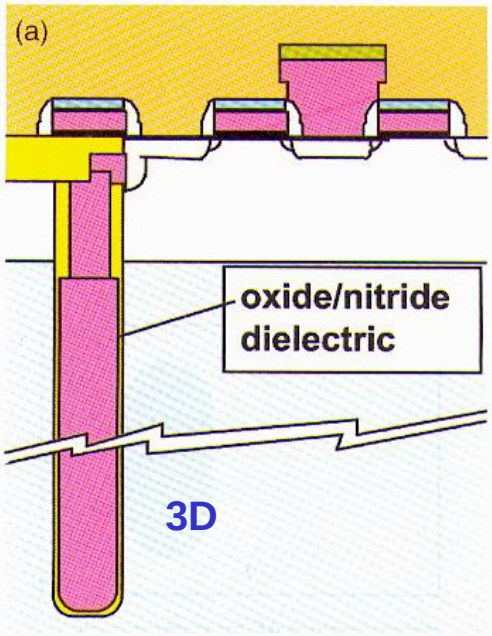
Figure 2: Schematic representation of a DRAM memory cell.

The value of the cell capacitance, C_S, varies only slowly with DRAM generation due to the same trends for the cell charge, Q_S, and the operating voltage, V_{DD}. For the 256 Mb chip, C_S is approx. 25 fF. The geometrical dimensions can be approximated very well by using the equation for the parallel plate capacitor:

$$C_S = \varepsilon_0 \varepsilon_r \frac{A_S}{t_{phys}} = \varepsilon_0 \varepsilon_{r,SiO_2} \frac{A_S}{t_{eq}} \quad \text{with } t_{eq} = \frac{\varepsilon_{r,SiO_2}}{\varepsilon_r} t_{phys} \text{ and } \varepsilon_{r,SiO_2} = 3.9. \qquad (1)$$

A_S is the total area of the capacitor, (defined by the surface area of the bottom electrode), t_{phys} is the physical thickness of the dielectric, and ε_r its relative permittivity, while ε_0 is that of vacuum. Eq. (1) also defines the equivalent dielectric thickness, t_{eq}, with respect to the relative permittivity of SiO_2, $\varepsilon_{r,SiO2} = 3.9$, as this dielectric was used at the beginning of DRAM history. With higher integration density, it was replaced by a mixture of Si oxide and nitride layers ($\varepsilon_{r,SiN}$ approx. 11) with higher effective dielectric constant, the so-called ON dielectric. Starting with the 4 Mb generation, the required capacitor area, A_S, was too large for the cell area, A_{CA}, and the cell capacitance could not be achieved with a planar geometry. Consequently, the third dimension had to be used in the form of trenches (see Figure 3) and later also of posts in a stacked geometry (see Figure 4).

C_S



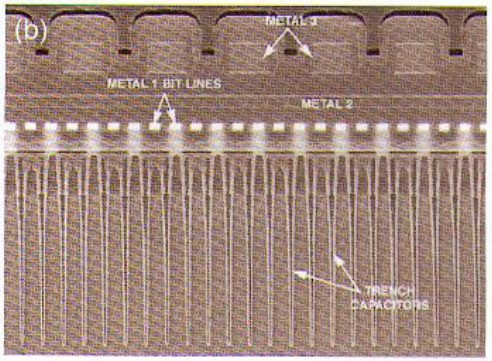
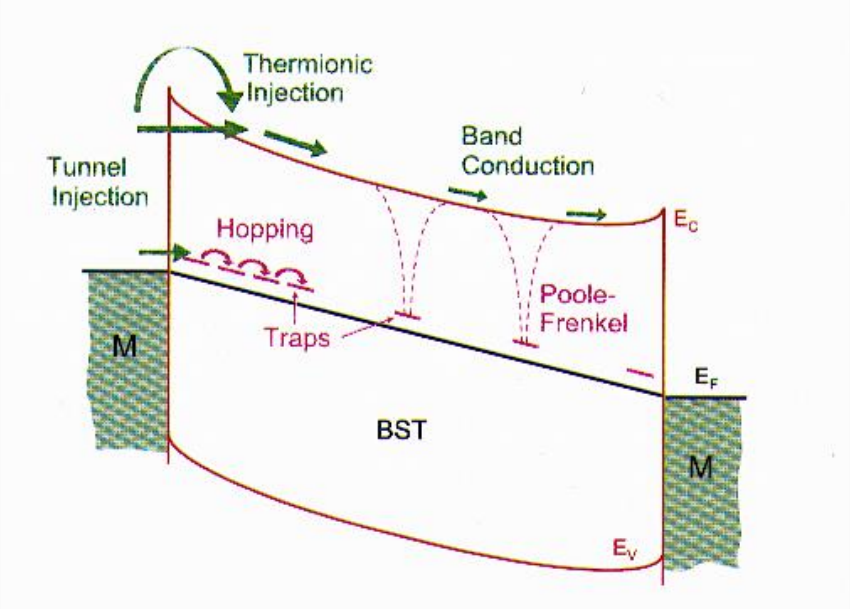


Figure 3: Example of a 3-D capacitor: (cross section) deep trench with oxide/nitride dielectric ($\varepsilon_r \approx 7$).
(a) Schematic, from [8];
(b) Scanning electron micrograph for Toshiba/ Infineon 64 Mb chip. The design is similar in 256 Mb and 1 Gb chips with much higher aspect ratios (height/ depth).

Capacitor material (oxide) and geometry become critical when reducing size

Da R. Waser Ed., Nanoelectronics and information technology (Wiley-VCH, 2003)

Problems/issues with the oxide material



Very thin dielectric layers can suffer conduction through several effects

3 Challenges for Gb DRAM Capacitors

Entering the Gb era, the capacitor of the DRAM cell in the conventional design is approaching its limits: (i) The thickness of the (Si) oxide/nitride (ON) compound layer allows no further thinning beyond approx. 5 nm because of unacceptably high tunneling leakage currents (see Sect. 5.2) reducing the stored capacitor charge to too low values, and (ii) the 3-D geometry is already very complicated and, hence, rather expensive due to the high number of processing steps. Some examples of very advanced 3-D structures are shown in Figure 3 (trench capacitor) and Figure 4 (stacked capacitor). Both have been produced with the 250 nm technology, i.e. the minimum feature size, F, was 250 nm, which was used when this generation was introduced into the market. The DRAM cell area, A_{CA}, was approx. $12\,F^2 = 0.75\ \mu m^2$ and the equivalent thickness, $t_{eq} = 5$ nm (see Eq. (1)), which corresponds to a physically thicker layer using ON dielectrics [9]. The challenges of the capacitor for future Gb DRAM generations will be demonstrated with the help of a detailed description of Figure 3 and Figure 4. Some important characteristic numbers for these capacitors will be summarized in Table 1 together with the respective ones for higher permittivity materials such as Ta_2O_5 ($\varepsilon_r \approx 22$) or (Ba,Sr)TiO_3 (BST) ($\varepsilon_r = 200$).

The most impressive feature of the trench capacitors shown in Figure 3b is their depth, more than 7 µm with 250 nm width at the top resulting in an aspect ratio (i.e. depth/width) of near 30. Thus, the necessary capacitor area, $A_S = 5.1\ \mu m^2$ corresponding to a capacitance of 35 fF, can be supplied. The projected area of the trench capacitor in the cell area is only $2\,F^2 = 0.125\ \mu m^2$ or 16 % of A_{CA} (see Figure 5a). The reason for this small fraction can be realized from the schematic representation of a trench cell in Figure 3a. The cell area has to be shared with the select transistor and the local wiring, the capacitor is in an offset position similar to the planar capacitors in early DRAM generations.

- ✓ Thin layers are needed to have enough capacitance with small surfaces (C~S/h)
- ✓ Thin layers are typically defective (polycrystalline!) and Poole-Frenkel or other effects can lead to conduction
- ✓ Search for new material with higher ε_R to increase the capacitance while keeping dimensions unaltered

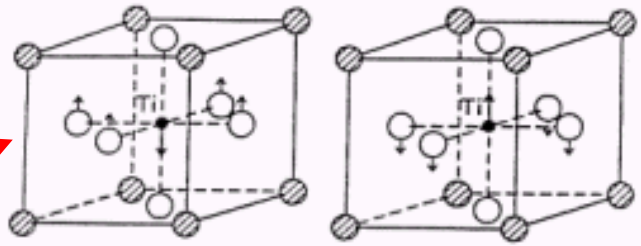
Requirements for suitable dielectrics (oxide)

The most relevant requirements are listed for a thin film dielectric with high permittivity to be integrated into a capacitor of a DRAM 1T-1C cell in a CMOS chip of an advanced Gb generation:

- Most important is a high permittivity ($\epsilon_r \geq 200$) to guarantee simpler electrode geometries, i.e. low 3-D folding factor, for several DRAM chip generations. A charge of about 25 fC at voltages ≤ 1 V has to be loaded to the cell capacitor. This corresponds to a usable cell capacitance $C_S \geq 25$ fF.
- The material has to be homogeneously deposited as a thin film with thickness of ≤ 30 nm over large areas (12" wafer size). The deposition method has to ensure a conformal coverage in order to coat 3-D structures. The thermal budget should be as low as possible. For these reasons, the metal-organic chemical vapor deposition (MOCVD) technique is most suited for the deposition (see also Chapt. 8).
- As the read and write times will approach 1 ns, the dielectric behavior should not show a significant dispersion up to frequencies of a few GHz.
- Refresh times of the order of 1 s are desirable. Within the refresh time, the charge loss due to polarization relaxation and leakage currents has to be smaller than 10%.
- Long-term stability of the properties (10 years is the projected lifetime) is indispensable.
- All the processes for the dielectric material itself as well as for the electrodes and the possibly necessary diffusion barrier and adhesion layers have to be compatible with the CMOS process technology.

These requirements will be discussed in the context of one of the most promising candidate materials, BST, which is a mixed oxide of the ABO_3 type with a perovskite crystal structure. It is derived from the ferroelectric $BaTiO_3$, but it does not show a ferroelectric hysteresis as a thin film on a Si substrate because (i) the solid solution of strontium on the barium "A" site shifts the Curie point to lower temperatures and (ii) the geometrical confinement as a thin film on a thick Si substrate leads to the typical biaxial tensile stress conditions on cooling from high processing temperatures (550°C to 750°C) to ambient temperatures if its thermal expansion coefficient is larger than that of Si. Rather, it behaves as incipient ferroelectric or superparaelectric film [10]. The properties of BST depend on the relative concentration of the components, especially on the ratio of Ba and Sr (the Ba:Sr ratio is about 70:30 in the films discussed in this section), and on the conditions of deposition and recrystallization treatment. Therefore, we report the properties from only a few sources to assure comparability of the different dependences.

BST:
Mixture of strontium and barium titanates



Perovskite ceramics with large static dielectric constant (~200) and negligible ferroelectricity

Can be deposited as thin film by MO-CVD

Flash memories

Flash Memory

Flash Memory, the most common non-volatile, programmable memory device, uses rows and columns of interconnects that address each data cell. At the intersection of these are two transistors, which comprise the Flash Memory cell, as shown in Fig. 30.9. Each cell is addressed by a network of interconnects, where the common connection to the transistor gates is called the word line and the common connection to the drain is called the bit line. Every cell in the memory array can be accessed by activating a unique combination of these lines. Here, the floating gate is linked to a word line via a second gate that serves as a control gate. The floating gate potential is altered by Fowler–Nordheim tunneling of electrons, an effect that takes place when the applied bias needed for switching is larger than the work function of the relevant electrode. The electrons arrive from the column, or bit line, and enter the floating gate from which they drain to the ground. A cell sensor monitors the flow of electrons through the gate. A value of 1 is assigned when the current is greater than a given threshold value, and 0 if it is below that value. Approximately 30,000 electrons are stored in the gate to make a 1 and 5,000 for a 0. The memory of the device derives from the very long storage time (tens of years) of the tunneling electrons in the gate capacitor. For the data to have a lifetime of ten years, the electrons can leak at a rate of no more than five a day. Flash memory can only be rewritten a limited number of times (10^{5-6}), as electrons get permanently trapped in the gate over time, impairing device efficiency. Memory devices using this technology are SmartMedia, Com-

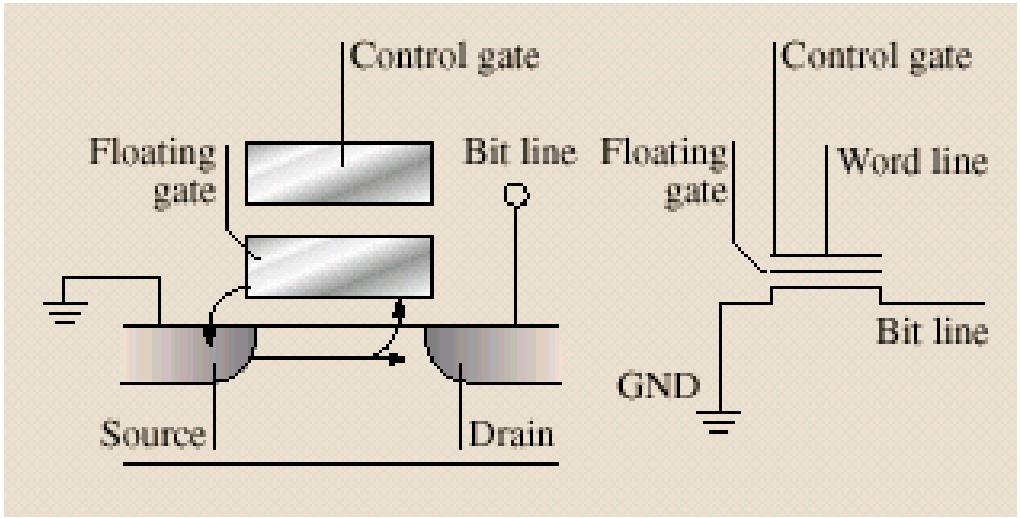


Fig. 30.9 Schematics diagram of a typical Flash Memory cell

Flash memories (e.g., smart card, SD, etc.) exploit charge retention in a floating gate

Fowler-Nordheim tunneling is used to change the charge status

Da B. Bhushan Ed., Springer Handbook of Nanotechnology (Springer, 2004)

Fowler-Nordheim tunneling

Field emission - also called Fowler-Nordheim tunneling - is the process whereby electrons tunnel through a barrier in the presence of a high electric field. This quantum mechanical tunneling process is an important mechanism for thin barriers as those in metal-semiconduictor junctions on highly-doped semiconductors.

We derive of the tunnel probability from the time independent Schrödinger equation:

$$-\frac{\hbar^2}{2m^*}\frac{d^2\Psi}{dx^2} + V(x)\Psi = E\Psi \qquad [3.1.44]$$

which can be rewritten as

$$\frac{d^2\Psi}{dx^2} = \frac{2m^*(V-E)}{\hbar^2}\Psi \qquad [3.1.45]$$

Assuming that $V(x)$-E is independent of position in a section between x and $x+dx$ this equation can be solved yielding:

$$\Psi(x+dx) = \Psi(x)\exp(-k\,dx) \quad \text{with } k = \frac{\sqrt{2m^*[V(x)-E]}}{\hbar} \qquad [3.1.46]$$

The minus sign is chosen since we assume the particle to move from left to right.For a slowly varying potential the amplitude of the wave function at $x = L$ can be related to the wave function at $x = 0$:

$$\Psi(L) = \Psi(0)\exp\left(-\int_0^L \frac{\sqrt{2m^*[V(x)-E]}}{\hbar}dx\right) \qquad [3.1.48]$$

This equation is referred to as the WKB (Wigner, Kramers, Brillouin) approximation. From this the tunneling probability, Θ, can be calculated for a triangular barrier for which $V(x)$-E = $q\phi_B(1-x/l)$

$$\Theta = \frac{\Psi(L)\Psi^*(L)}{\Psi(0)\Psi^*(0)} = \exp\left(-2\int_0^L \frac{\sqrt{2m^*}}{\hbar}\sqrt{q\,\phi_B\left(1-\frac{x}{L}\right)}\,dx\right) \qquad [3.1.49]$$

the tunneling probability then becomes

$$\Theta = \exp\left(-\frac{4}{3}\frac{\sqrt{2qm^*}}{\hbar}\frac{\phi_B^{3/2}}{\mathcal{E}}\right) \qquad [3.1.50]$$

where the electric field equals $E = \phi_B/L$.

The tunneling current is obtained from the product of the carrier charge, velocity and density. The velocity equals the Richardson velocity, the velocity with which on average the carriers approach the barrier while the carrier density equals the density of available electrons multiplied with the tunneling probability, yielding:

$$J_n = q v_R n \Theta$$

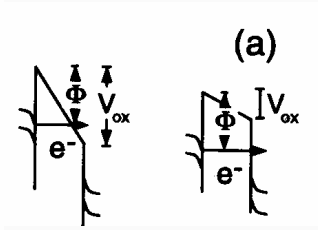
The tunneling current therefore depends exponentially on the barrier height to the 3/2 power.

http://ece-www.colorado.edu/~bart/book/msfield.htm

For voltages larger than 4 V and $t_{ox} < 5$ nm, the current is described by Fowler-Nordheim tunneling[73–75] while direct tunneling is observed for voltages < 4 V; the physical distinction between the two is illustrated by Figure 12. Direct tunneling (DT) presents a trapezoidal barrier to tunneling with a field independent thickness, whereas Fowler-Nordheim tunneling (FN) presents a triangular barrier with a thickness that depends on the applied voltage. If we ignore, for mathematical economy, the depletion of the polysilicon gate and the quantum mechanical thickness of the inversion layer, and assume that the gate voltage is entirely dropped across the insulator, the current density in the DT regime can be written as:

$$J = \frac{AF_{ox}^2}{[1-(1-qV_G/\phi)^{1/2}]^2}\exp\left[\frac{8\pi\sqrt{2m_{ox}}\,\phi^{3/2}}{3hqV_G}\left((1-qV_G/\phi)^{3/2}-1\right)t_{ox}\right] \quad (14)$$
$$= \frac{AF_{ox}^2}{[1-(1-qV_G/\phi)^{1/2}]^2}\exp\left[\frac{\phi\left((1-qV_G/\phi)^{3/2}-1\right)}{qV_g}\frac{t_{ox}}{\Lambda}\right],$$

where A is a constant, $\Lambda = 4\sqrt{2m_{ox}\phi}/3\hbar \approx 0.1-0.2nm$ is the evanescent decay length of the electron, $F_{ox} = V_G/t_{ox}$ is the field in the insulator, ϕ is the barrier height, and m_{ox} is the effective mass in the oxide bandgap. The barrier height and the effective mass are usually determined empirically by a fit of Eq. (14) to experimental data; typically for thick barriers $\phi \approx 3.1-3.2\ eV$ and $m_{ox} \approx 0.42-0.38m_e$, where m_e is the free electron mass. For high fields $qV_G = \phi$, the familiar Fowler-Nordheim (FN) equation for tunneling is recovered from Eq. (14), but in the DT regime the current is enhanced over the FN prediction, owing to the seemingly insignificant change in the barrier from triangular to pezoidal[71]. The current enhancement still shows an exponential dependence



FN DT

FN vs DT

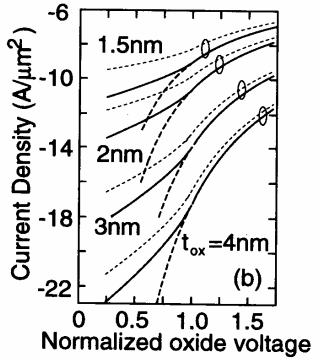


FIGURE 12. (a) The potential barrier in an insulating film between two electrodes for $V \approx 0$, $V < \phi_o/q$; and $V > \phi_o/q$. (b) The tunneling current through a large (≈100 μm ×100 μm) MOS capacitor structure as a function of the applied voltage normalized by the barrier height, ϕ for t_{ox} = 1.5, 2, 3, and 4 nm. No accounting is made for the depletion of the polysilicon gate or the quantum mechanics of the inversion layer. The solid lines result from a calculation in which interfaces are atomically smooth, while the dotted lines represent the same calculation assuming Gaussian roughness of 0.25 nm-rms at one interface. The dashed lines indicate the current due to Fowler-Nordheim tunneling alone without direct tunneling. The same prefactor for the tunneling current is used for all of the calculations and it is made to be consistent with experimental data obtained from a 3nm oxide.

Fowler-Nordheim: tunneling (at high bias) through triangular barrier whose height depends (slightly) on the bias itself

Da G. Timp, Nanotechnology (Springer-Verlag, 1999)

Micro vs nano comparison in the RAM/flash world

See R. Compaño et al.
MEL-ARI EC Project
Technol. Rodmap 1999

Charge stored in a quantum dot with possible single electron behavior

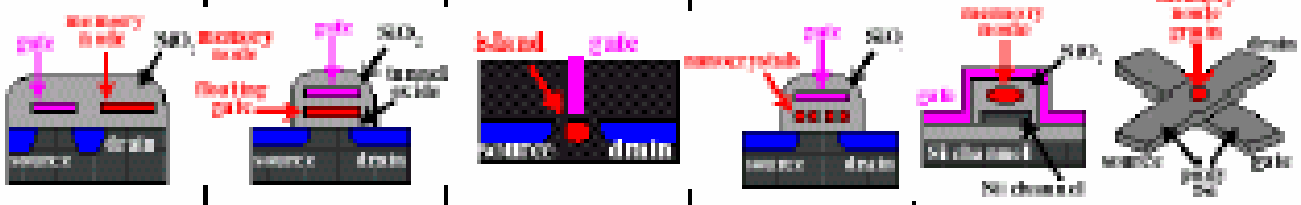
	Conventional Memory		Quantum Dot Memory			
	DRAM	Flash	SET	Nano-flash		Nano-type
				Multidot	Single dot	
device structure						
read time	~10 ns	~10 ns	1 ns	~10 ns	~10ns	~20 μs
write time	~10 ns	~1 ms	1 ns	~100 ns	<1 μs	~10 μs
erase time	< 1ms	~1ms	< 1ns	~1 ms	<1 ms	~10 μs
retention time	~1 s	~10 years	~ 1s	~1 week	~5 s	~1 day
endurance cycles	infinite	10^{4}	infinite	10^{5}	10^{5}	10^{5}
operating voltage	3 V	15 V	1 V	5 V	10 V	15 V
voltage for state inversion	0.2 V	~5 V	< 0.1 V	0.65 V	0.1 V	0.5 V
electron number to write bit	10^{5}	10^{5}	1 (excluding ne to change gate potential)	10^{5}	1 (excluding ne to change gate potential)	2 (excluding ne to change gate potential)
cell size	~12 F²/bit	~8F²/bit	9-12 F²/bit	9F²/bit	9F²/bit	2F²/bit

Table 2.1:- Performance comparison among conventional and proposed memories (modified after data from Hitachi Cambridge Laboratory). For complete overview see table I.1 in Annex I

Examples of nanosized memories (proposed)

See R. Compaño et al.
MEL-ARI EC Project
Technol. Rodmap 1999

2.2.1.2 Nano-flash device

Nano-flash devices are basically three terminal devices where a floating gate is charged and the charge produces a large change in the threshold voltage of the transistor channel. The design allows an intermediate between DRAM and Coulomb blockade potentially allowing higher density than DRAM at lower power and higher operating temperatures.
In addition, nonvolatile Dram-like memories based on the Coulomb blockade effect are intensively investigated. Both Hitachi's PLED [Nakazato 1997] and Likharev's NOVORAM being [Likharev 1998] are prominent examples. The key issue is the creation of extremely flexible tunnel barriers, for instance by multiple barriers or sandwiched barriers.

2.2.1.3 Yano memory (they can be fabricated by the "undulated" technology we have seen for quantum dots)

The Yano type memory is a 2 terminal device where information is stored in deep traps in poly-Si. The devices are created on a 3 nm thick Si film using 0.25 µm technology where one or more dots are formed naturally in the vicinity of a FET in which trapped charge modulates the threshold voltage of the FET [Yano 1998]. The device can be operated at room temperature and has been integrated in very large-scale memories (128 Mb in 8k x 8k x 2 units of which half was operational) although it is not certain if Coulomb blockade is of any relevance for device operation. One of the major problems of this type of memory is relying on the natural formation of dots and the resulting poor control of device characteristics. This may be a major hurdle to manufacturability [Yano 1998]. The advantage is a small cell size of 2F2, one quarter of a folded-data line DRAM cell size.

Coulomb blockade, or, more in general, quantum dots can be used to store the charge

Fundamental limits in miniaturization

2.1.1 Theoretical Limits

In order to understand the theoretical limits of information storage, it is useful to place CMOS in the context of a general purpose computation system. There are three important limits, which determine the ultimate performance of such systems. These limits are the thermal limit, the quantum limit, and the power dissipation limit (see figure 2.1). The energy necessary to write a bit determines the thermal limit. This energy must be bigger than the average energy of the thermal fluctuations, kT, otherwise bit errors will occur. For CMOS, the energy necessary to write a bit is about 10^{-13} J (10^{6} eV) which corresponds to a temperature of 10^{10} K. The trend in CMOS is to decrease this energy and thereby decrease the power dissipated. The optimum value for the energy to write a bit for room temperature operation is about 4×10^{-19} J (2 eV), which is one hundred times greater than kT.

The energy needed to read or write a bit and the frequency of the circuits are limited by the uncertainty principle, $\Delta E\ \Delta t \geq h$. To prevent bit errors, the circuit cannot operate too close to the minimum uncertainty product. The quantum limit is then approximately given by $E/f = 100\ h$ where E is the energy needed to write a bit and f is the clock frequency. CMOS circuits operate far above the quantum limit but as scaling continues below 100 nm, the limit will eventually be approached as E decreases and f increases (See Table 1).

The next important limit is the power dissipation limit, determined by the power density $p = EfnP$, where n is the device density, and P the probability that the device switches in a clock cycle, typically $P \sim 0.1$. The maximum tolerable power density is about 100 W/cm^2. This means that the energy, the frequency, and the packing density are limited by $Efn \sim 100$ W/cm^2. At high frequency, a high device density is desirable, and therefore a low energy per bit is desirable. CMOS circuits operate near the power dissipation limit. These three limits can be summarised in an energy - delay diagram as shown in figure 2.1.

Major limits:

- ✓Thermal
- ✓Quantum
- ✓Dissipative

See R. Compaño et al.
MEL-ARI EC Project
Technol. Rodmap 1999

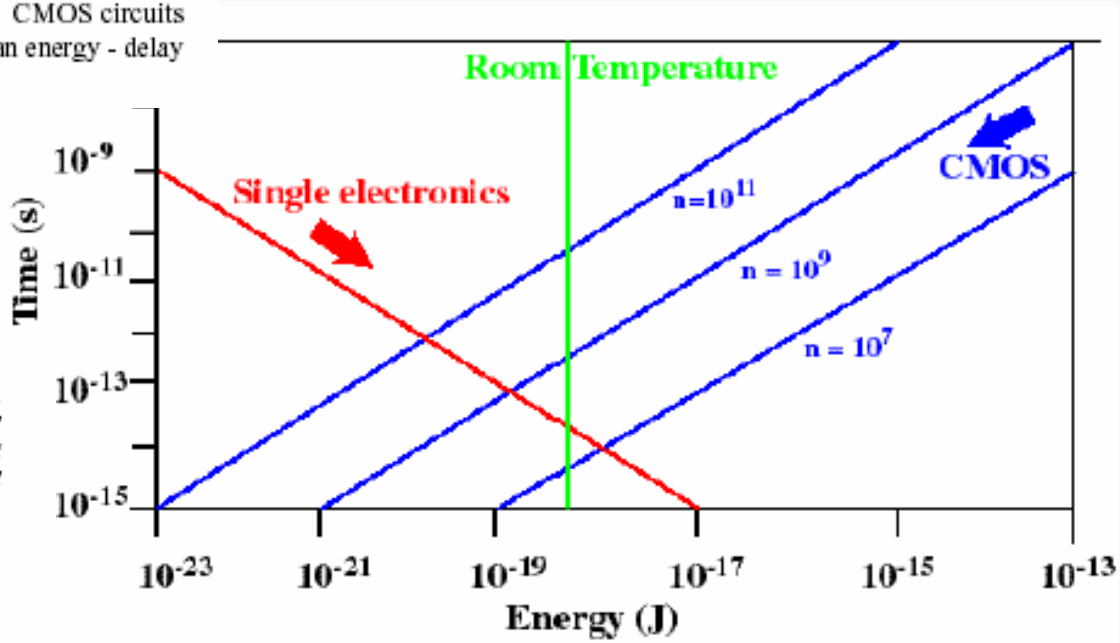


Figure 2.1:- An energy - delay diagram for single electronics. Room temperature operation can only be achieved to the right of the line labelled room temperature. The lower left-hand corner of the diagram is inaccessible due to quantum fluctuations and the lower right-hand corner of the diagram is inaccessible due to dissipation. The dissipation limit is represented by three lines, each corresponding to a different device density, n. The current trends in CMOS and single electronics are indicated in the diagram [Hadley 1996].

Non-volatile RAM with ferroelectric materials

Ferroelectric properties

Ferroelectrics are a class of material with polarisation dipoles that can be re-orientational by a sufficiently strong external electric field. Polarisation is defined as the charge per unit area on a plane orthogonal to the direction of the polarisation vector and has units of Cm^{-2}. The magnitude and orientation of the polarisation vector, P, is dependant on the magnitude and orientation of the electric field E and the crystal structure of the sample being poled. Hysteresis arises from the energy required to reverse the dipole, as positive and negatively polarised dipoles have the same energy. Energy dissipated during polarisation reversal is equivalent to the area of the loop. Figure 1 shows the relationship of P against E.

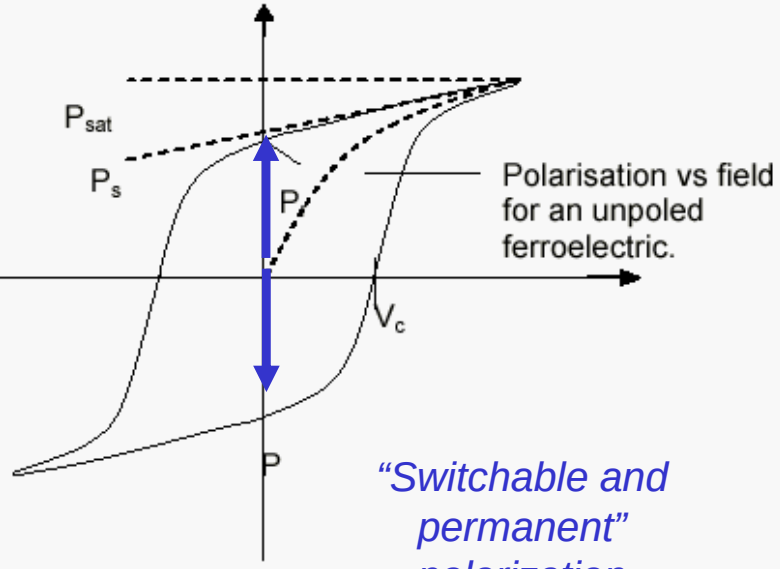


Figure 1 Ferroelectric polarisation loop

E = V/d

⇩

Thin films!!

"Switchable and permanent" polarization

Ferroelectricity allows information (charge) storing without an applied field

⇩

- New materials
- New thin film techniques

Ferroelectric ceramics (e.g., PZT)

Il più semplice tipo di prototipo ferroelettrico è la struttura centrosimmetrica perovskitica, caratteristica, per esempio, del $PbTiO_3$. Esso presenta una transizione alla fase ferroelettrica (che avviene in modo discontinuo) alla temperatura di 493 °C, con una deformazione della struttura da perovskitica a tetragonale. La fase polare è stata ricondotta allo spostamento dello ione Ti^{4+} verso uno degli atomi di ossigeno, disposti ottaedricamente attorno ad esso (Fig. 1.8).

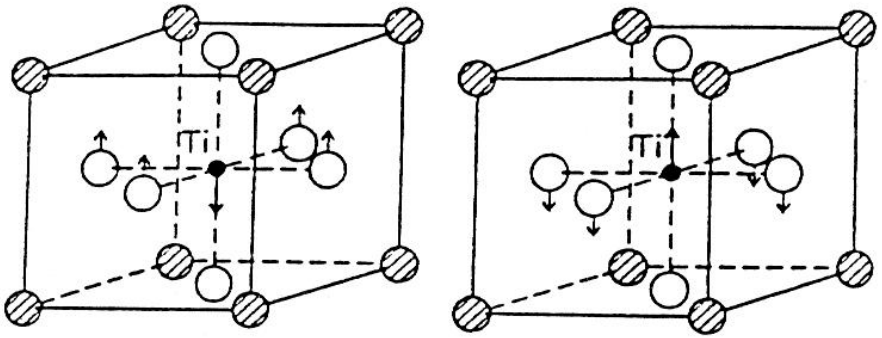
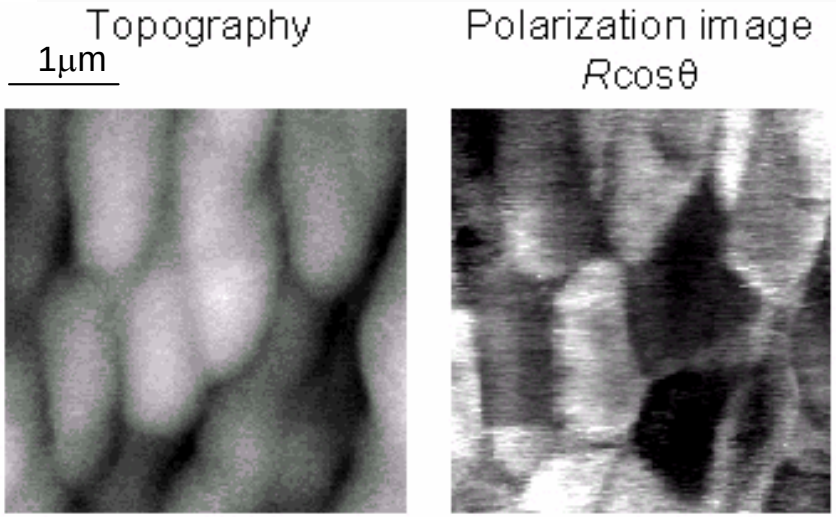


Figura 1.8: Deformazione della struttura del titanato di piombo da perovskitica a tetragonale. Da [18].

Ceramic oxides (or oxide mixtures) with perovskite structure



Polarization due to charge displacement in a quasi-ionic crystal

AFM/EFM (Voltage modulation scanning probe microscopy) of ferroelectric domains in films of (lead lanthanum titanate) grown by PLAD

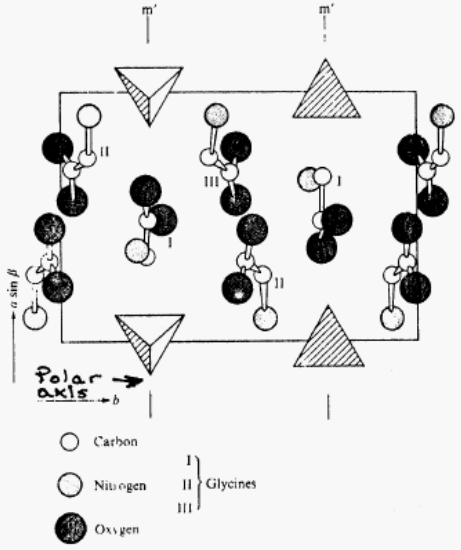
See http://www.df.unipi.it/gruppi/struttura/ma/page.htm

Molecular ferroelectrics (e.g., TGS,…)

TriGlycine Sulfate (TGS)

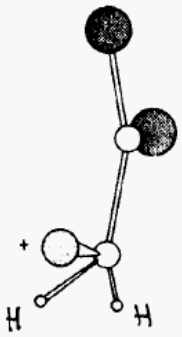
The crystals of TGS you are given have been grown from an aqueous solution by slow evaporation. The solubility curve that makes this possible is shown in Figure 1. The morphology of the crystals is shown in Figure 2. The crystal structure is complex and of fairly low symmetry (monoclinic). The mechanism by which the spontaneous dipole moment is created is also complex and is not yet fully understood. However, crudely speaking, the glycine molecule I in Figure 3 on average lies on a plane of mirror symmetry in the structure at $T \geq T_c$ and there is no net dipole moment. We say the structure is "centrosymmetric" in its high-temperature phase. For $T < T_c$ on the other hand, the nitrogen atoms in the glycine molecules are found to be displaced to the left (or right) of the mirror plane, along the polar axis b. Thus a dipole moment is set up in each unit cell. The co-operative displacement of all such nitrogen ions in the sample thus produces a macroscopic dipole moment in much the same way that unpaired spins co-operatively align to create a magnetic moment in e.g. iron.

Struttura monoclina



(a)

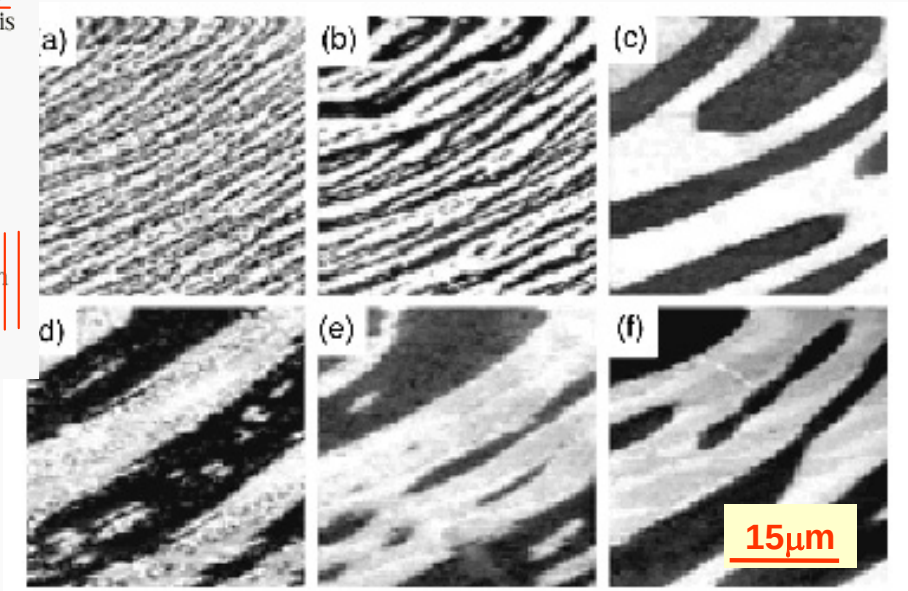
Glicina



$H_2NCH_2CO_2H$

(b)

Figure 3. View along the c-axis of the structure of TGS (after Hoshino, Okaya and Pepinsky, 1959; Itoh and Mitsui 1973) showing the three glycine groups I, II, and III. The suplhate ions are shown as tetrahedral. m and m′ are mirror planes in the high temperature phase.



EFM images of ferroelectric domains in TGS films at increasing temperatures

See Adv Phys Lab, Univ Michigan (2002)

Storage by magnetic means (e.g., hard-disk)

Magnetic polarization switching (parallel/antiparallel dipoles) of the ferromagnetic domains is a quite diffused method for data storage

Old implementations (non miniaturized!): ferrite nucleis and tape recording

Highly non volatile, scalable size (we will see problems later on!)

But read/write operation is not very efficient (magnetic fields are needed)

Presently: hard-disk, but also **magnetoresistive memories (MRAM)**

Nanostructured materials with giant magnetoresistance

Magnetoresistive materials: electrical resistance depends on applied magnetic field

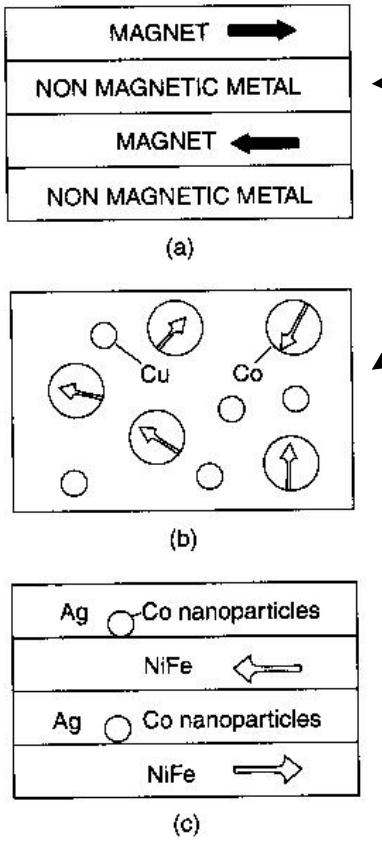


Figure 7.15. Three arrangements for producing colossal magnetoresistance: (a) layers of nonmagnetic material alternating with oppositely magnetized (arrows) ferromagnetic layers; (b) randomly oriented ferromagnetic cobalt nanoparticles (large circles) in a nonmagnetic copper matrix (small circles); (c) hybrid system consisting of cobalt nanoparticles in a silver (Ag) matrix sandwiched between nickel–iron (NiFe) magnetic layers, with alternating magnetization indicated by arrows.

Layered structures (alternate magnetic non magnetic layers), or nanosized domain dispersion, or mixed systems

Magnetoresistenza due to the sensitivity on magnetic field of the electronic scattering (see Drude) associated with magnetic polarization of layers or nanoparticles

Dispersed nanodomains (size ~ λ_{dB} of charge carriers)
enhance magnetoresistance

Poole, Owens, Introd. to nanotechnology (wiley, 2003)

Proposal of Magnetic RAM (MRAM)

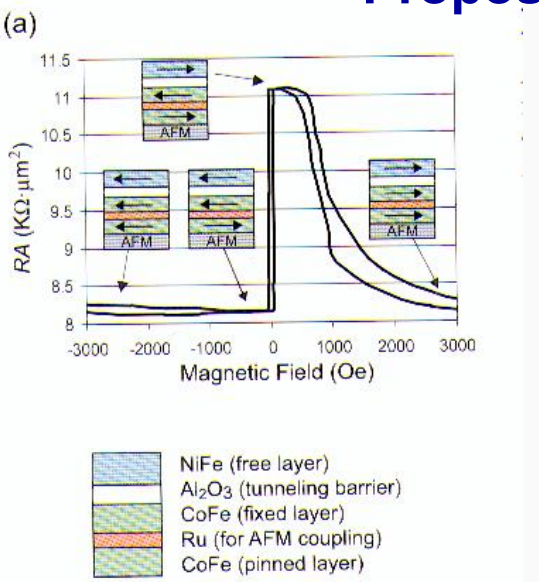
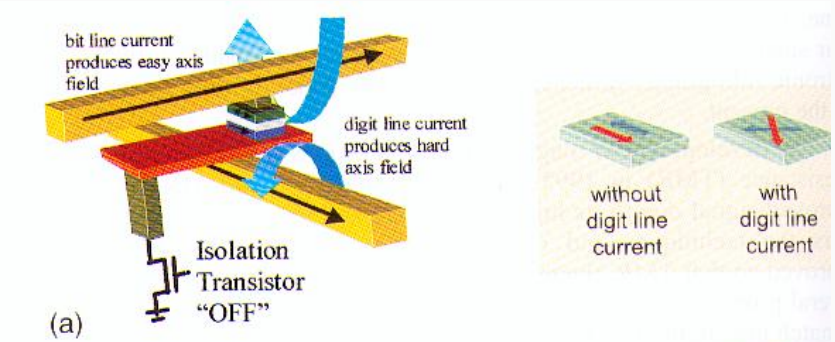


Figure 1: Resistance area product vs. external magnetic field of TMR stacks. The AFM layer pins the magnetization of the lowermost CoFe layer (*pinned layer*). The pinned layer is strongly antiferromagnetically coupled to the second CoFe layer (*fixed layer*) through a non-magnetic Ru layer (red). On top of the Al_2O_3 tunnelling barrier there is a NiFe layer that can be switched relatively easily. The magnetic layers show a thickness of 2 to 6 nm, the Ru layer of 0.7 to 0.9 nm.
(a) Characteristics of the TMR material (10 x 10 μm^2 bit).
(b) Characteristics of a 0.6 x 1.2 μm^2 TMR device.



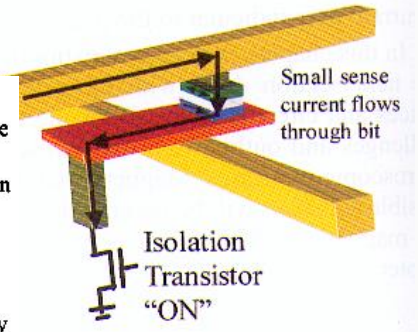


Figure 2: TMR bit stack placed at the crossing point of a bit line and a digit line. The magnetic moment of the fixed layer (blue) does not move in the applied field while the free layer (green) can be switched between two states.
(a) Single MRAM cell in "Write" Mode. Current in the bottom conductor (digit line) provides a field in the hard axis direction leading to a titling of free layer magnetization, as shown in the inset. This hard axis field lowers the easy axis field, provided by the top conductor (bit line), required to switch the bit. Only the bit in the array that experiences both hard and easy axis fields will switch. The isolation transistor is turned off during the write operation. Inset: Without a digit line current, the magnetization (red and blue arrows) is along the long axis of the rectangular shaped free layer (green), while a digit line current leads to a tilting of the magnetization directions which assists the switching procedure.
(b) Single MRAM cell in "Read" Mode. The top conductor is in contact with the top electrode of the TMR device. When the isolation transistor is turned on, a small sense current may flow from the top conductor, through the bit, and to ground.

Reading exploits magnetoresistance

Perspectives in mass storage (hard-disks)

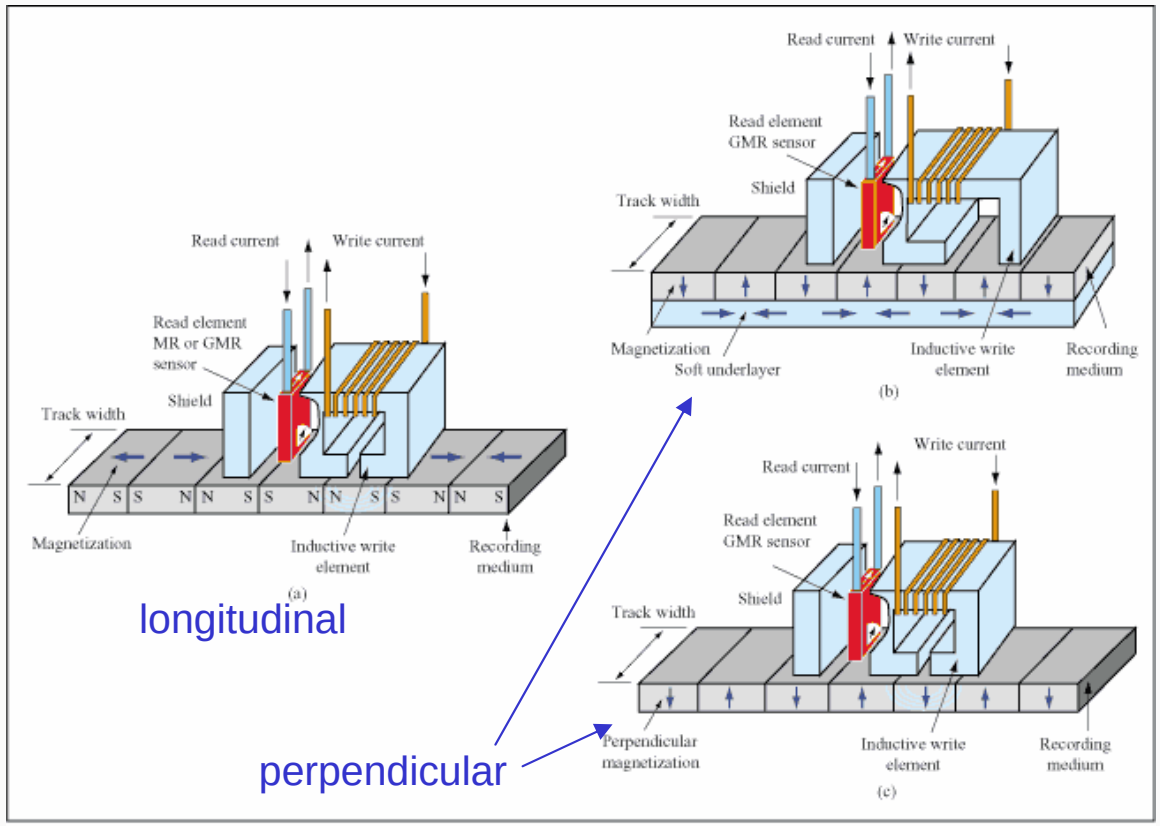


Figure 9

(a) Longitudinal magnetic recording. (b) Type 1 perpendicular recording, using a probe head and a soft underlayer in the medium. (c) Type 2 perpendicular recording, using a ring head and no soft underlayer.

Isolated domains dispersed in a matrix (magnetic grains – ferrous alloy, or NiCr, Co - islands)

Miniaturization -> surface density increase of domains

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Magnetic nanodomains

Thompson, Best, IBM J Res Dev (2000)

MFM image

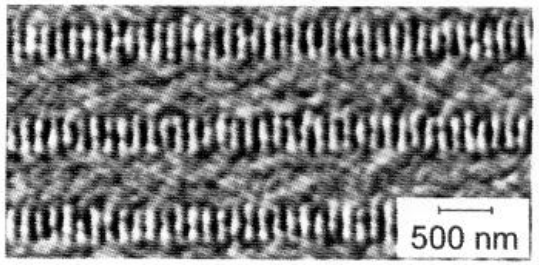
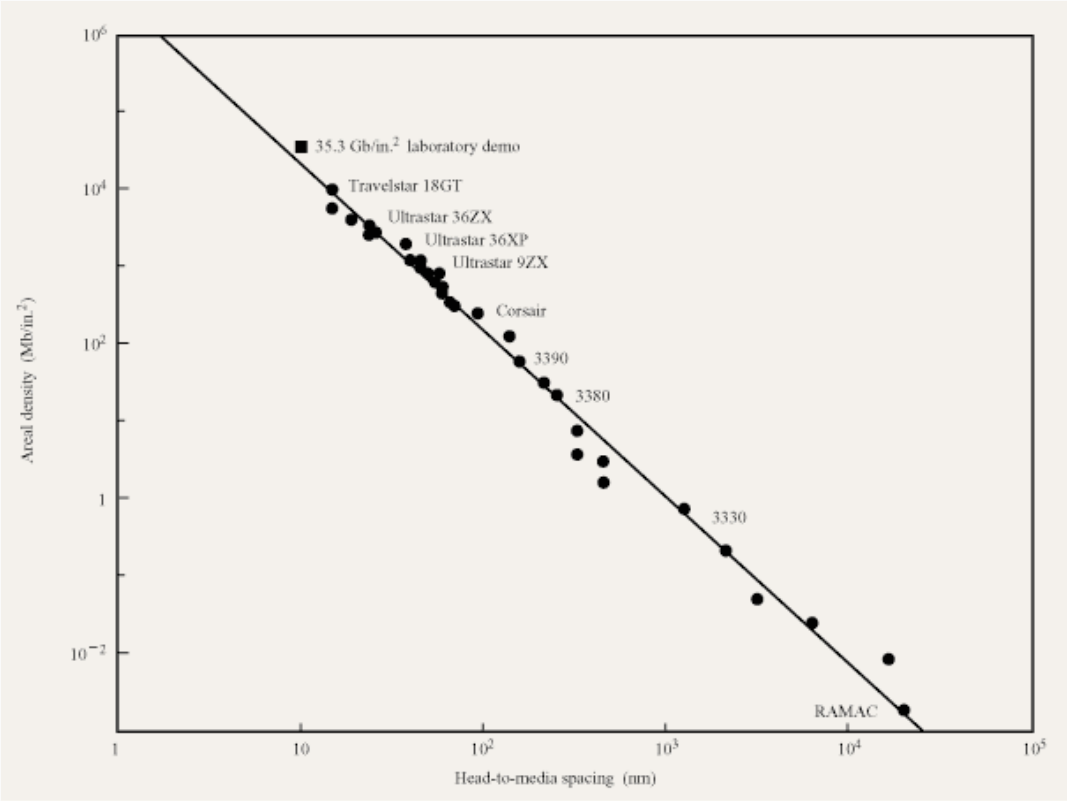


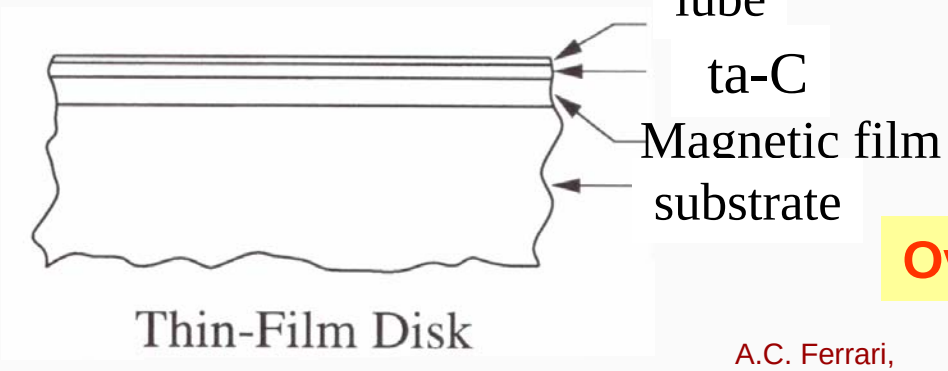
Figure 1: Magnetic force micrograph (MFM) of recorded bit patterns. Track width is 350 nm. The tracks are written at a frequency (linear bit density) slightly lower than used in the actual HDDs and every second track is skipped in order to give a clearer image.

Mechanical issues



Good S/N ratios in reading achieved only for **nanometer head/disk distance**

Overcoat requirements	Material requirements
• Reduce corrosion • Reduce friction • Reduce stiction • Reduce wear • Magnetically inert • Thermal management • Electrical isolation	• Dense pinhole free film • High hardness and E modulus • Eliminate surface roughness • Enhance surface chemistry

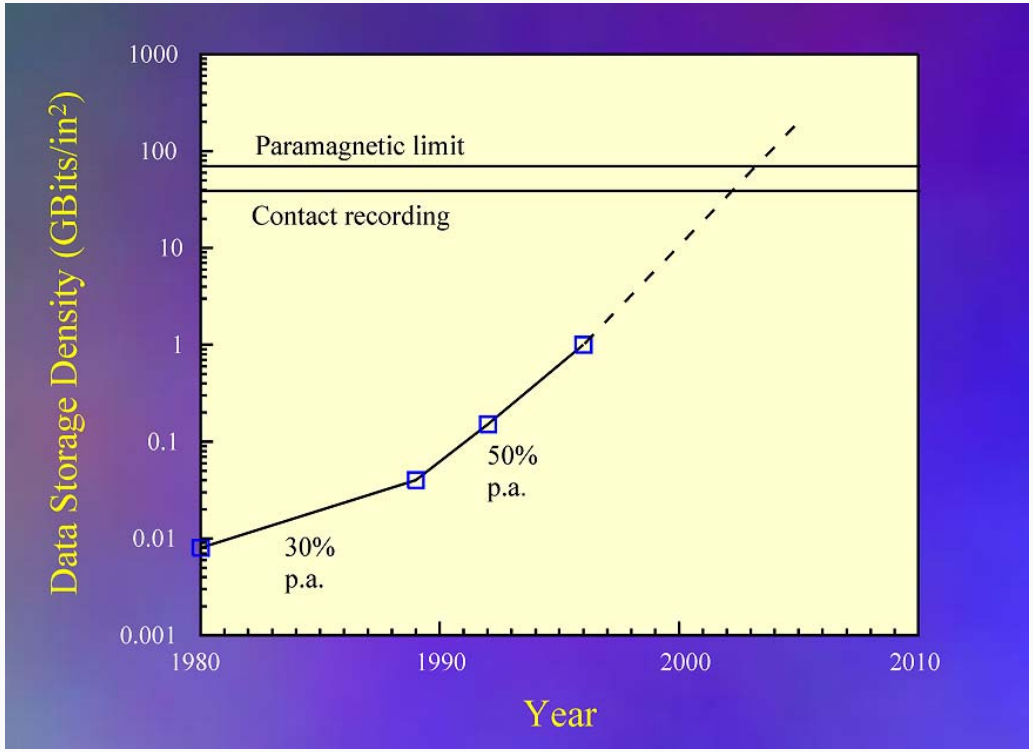


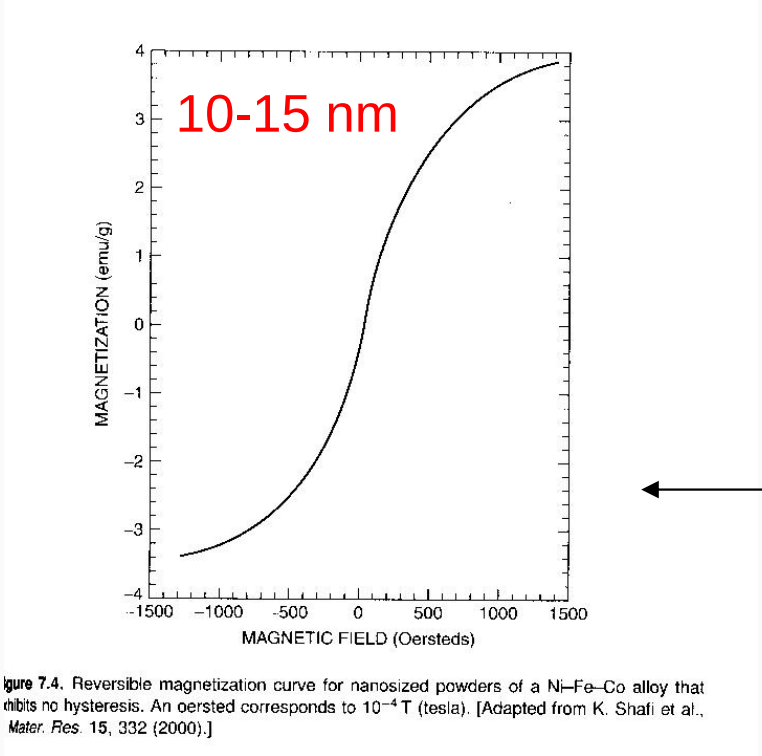
Overcoating technology highly demanding

A.C. Ferrari,
Cambridge University

Superparamagnetic materials I

Hard-disk magnetic materials evolved from sprayed tapes to superparamagnetic nanoparticles (materials with poor hysteresis and large remnant polarization)





igure 7.4. Reversible magnetization curve for nanosized powders of a Ni–Fe–Co alloy that hibits no hysteresis. An oersted corresponds to 10^{-4} T (tesla). [Adapted from K. Shafi et al., *Mater. Res.* **15**, 332 (2000).]

y powders of $Fe_{69}Ni_9CO_2$ having grain sizes of 10–15 nm prepared by decomition of solutions of $Fe(CO)_5$, $Ni(CO)_4$, and $Co(NO)(CoO)_3$ in the hydrocarbon vent decalin ($C_{10}H_{18}$) under an inert-gas atmosphere showed almost no hysteresis

Poole, Owens, Introd. to nanotechnology (wiley, 2003)

Superparamagnetic materials *II*

7.3 Self-Organized Particle Media

Recently, a new recording material approach based on self-assembling FePt nanoparticles has been reported [19]. The nanoparticles are chemically synthesized as indicated in the insert of Figure 24 by the reduction of platinum acetylacetonate and decomposition of iron pentacarbonyl. Their size and composition can be precisely controlled. When the particles are spread out on a substrate the carrier solvent can evaporate and the particles self-assemble into an ordered lattice with controlled spacing as is demonstrated by the micrograph in Figure 24. An annealing process transfers the internal particle structure into a chemically ordered face-centered tetragonal phase whereby ferromagnetic nanocrystals are formed. The annealed nanocrystal assemblies are smooth ferromagnetic films which can be considered as recording medium. The particle size is tunable from 3 to 10 nm with a standard deviation below 5 %. Compared to standard recording media the grain size distribution is very narrow. Therefore the number of grains per bit could be significantly reduced and optimized ferromagnetic nanocrystal superlattices can be considered as potential future storage media.

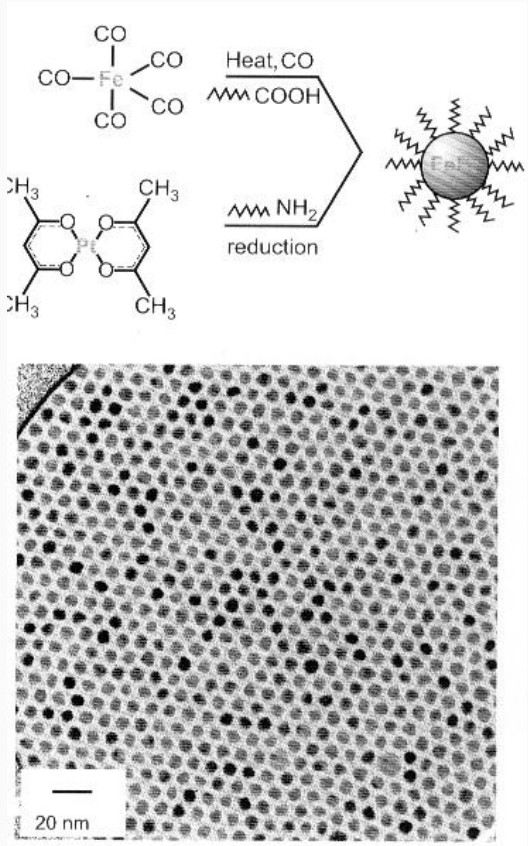


Figure 24: TEM micrograph of self assembled FePt nanoparticles (bottom). The schematic illustrates the fabrication roots for this self-assembled material (top) [19].

Self-organization of nanoparticles by (metallorganic) chemistry methods to enhance surface density

The superparamagnetic limit

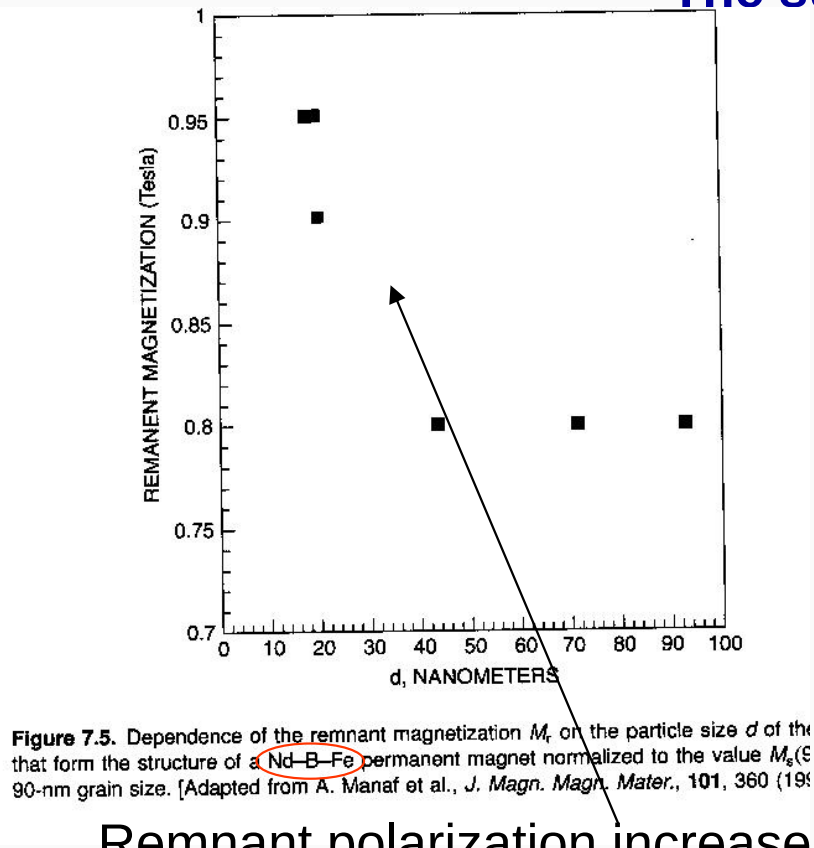


Figure 7.5. Dependence of the remnant magnetization M_r on the particle size d of the that form the structure of a Nd–B–Fe permanent magnet normalized to the value M_s(9 90-nm grain size. [Adapted from A. Manaf et al., *J. Magn. Magn. Mater.*, **101**, 360 (19

Remnant polarization increases as size decreases, but "associated energy" decreases as well

⇩

Superparamagnetic limit

Consider the simplest sort of permanent magnet particle. It is uniformly magnetized and has an anisotropy that forces the magnetization to lie in either direction along a preferred axis. The energy of the particle is proportional to $\sin^2$, where is the angle that the magnetization makes to the preferred axis of orientation. At absolute zero, the magnetization lies at one of two energy minima (equals 0 or 180°, logical zero or one). If the direction of the magnetization is disturbed, it vibrates at a resonant frequency of a few tens of gigahertz, but settles back to one of the energy minima as the oscillation dies out. If the temperature is raised above absolute zero, the magnetization direction fluctuates randomly at its resonant frequency with an average energy of kT. The energy at any time varies according to well-known statistics, and with each fluctuation will have a finite probability of exceeding the energy barrier that exists at = ±90°. Thus, given the ratio of the energy barrier to kT, and knowing the resonant frequency and the damping factor (due to coupling with the physical environment), one can compute the average time between random reversals. This is an extremely strong function of particle size. A factor of 2 change in particle diameter can change the reversal time from 100 years to 100 nanoseconds. For the former case, we consider the particle to be stable. For the latter, it is a permanent magnet in only a philosophic sense; macroscopically, we observe the assembly of particles to have no magnetic remanence and a small permeability, even though at any instant each particle is fully magnetized in some direction.

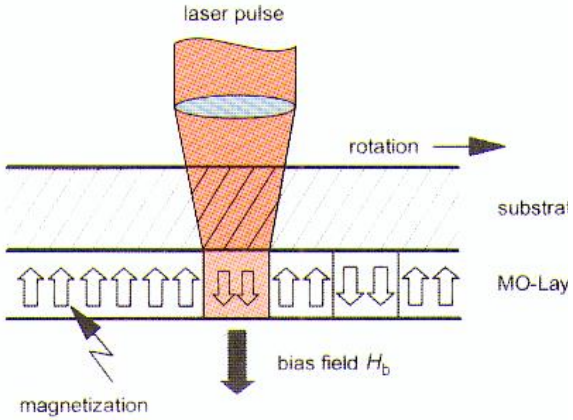
Present "theo" density ~ 25 Gb/cm²
Actual max density ~ 5 Gb/cm²

Magneto-optical methods

2 Principle of Magneto-Optical Data Storage

The **thermomagnetic writing process** used in the MO media is shown in Figure 1. A magnetic layer, which is homogeneously magnetized in one direction perpendicular to the surface, is heated by the laser pulse to a sufficiently high temperature where the coercivity H_c of the magnetic layer becomes smaller than a simultaneously applied bias field H_b. By this process a small domain is created whose magnetization is opposite to the original magnetization direction. As a result small bubble domains with magnetization down are formed in an environment with magnetization up. The two different magnetizations can be attributed to the binary numbers 1 or 0.

For read-out, the laser is operated with a sufficiently low power so that it does not change the domain structure. The polarization of the reflected light is then influenced by the magnetizations of the different domains due to the **magneto-optical Kerr effect (MOKE)**. When linearly polarized light is reflected from a sample with magnetization M perpendicular to the surface the polarization becomes elliptical with a small tilt (Kerr rotation) $\theta_K \leq 0.5$ degree, which is proportional to the magnetization (Polar Kerr effect, Figure 2a). In particular, $= \theta_K$ is obtained for opposite magnetization directions. By



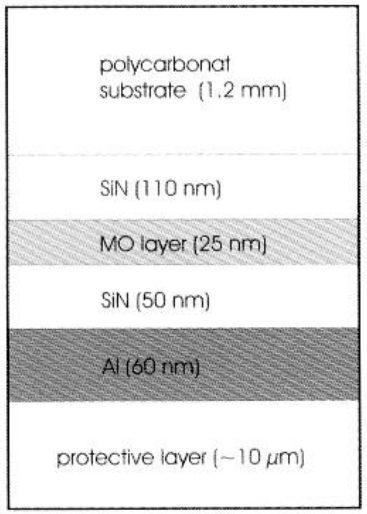


Figure 4: Layer stack of a typical MO disc [2].

Space resolution affected by optical diffraction

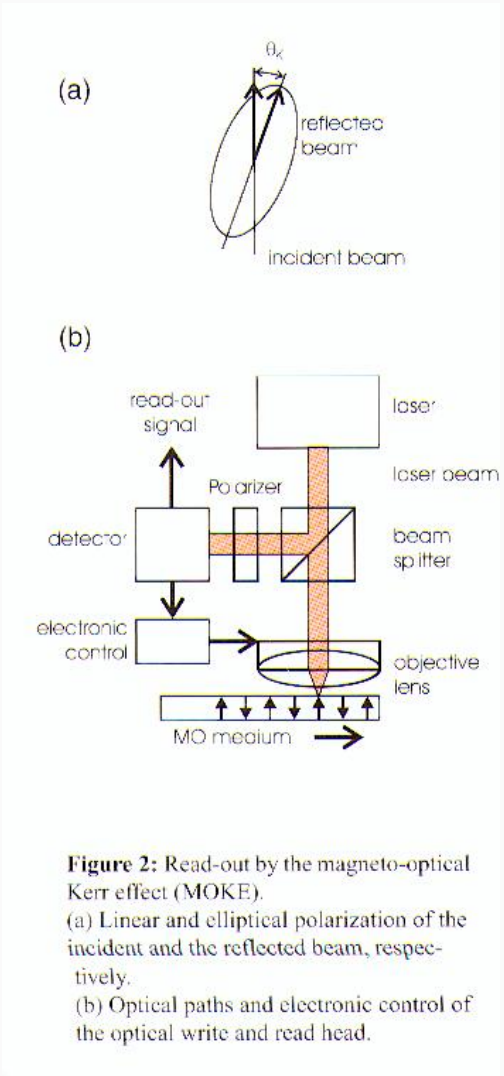


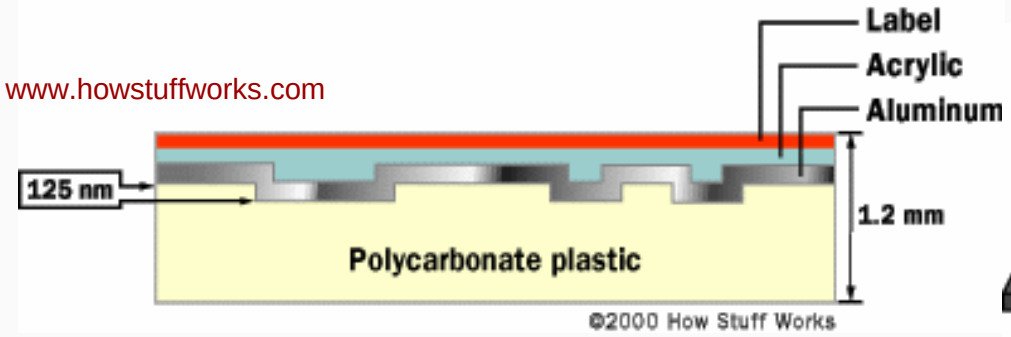
Figure 2: Read-out by the magneto-optical Kerr effect (MOKE).
(a) Linear and elliptical polarization of the incident and the reflected beam, respectively.
(b) Optical paths and electronic control of the optical write and read head.

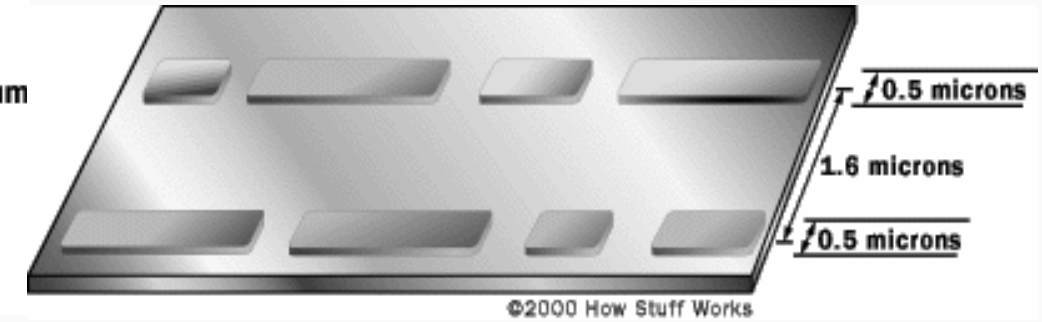
Light polarization is used for reading (possible improvements of S/N)

Optical data storage (CD-ROM, CD-RW, DVD,...)

Basic motivations (hystorical): economy, density, immunity from spurious agents

Optical methods allow displacing the read/write head far from the (rotating) disk, improving size reduction and mechanical reliability

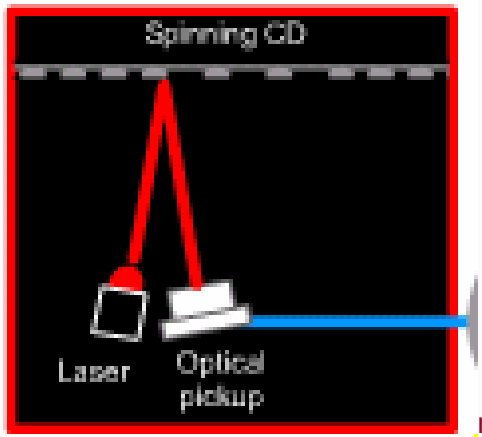




CD-ROM (original design): bits are “holes” impressed in a reflecting Al film evaporated onto a polycarbonate substrate

Writing: master mechanically impressed onto the Al film (**no re-writable!)**

Reading: deflection of a (focused) laser beam

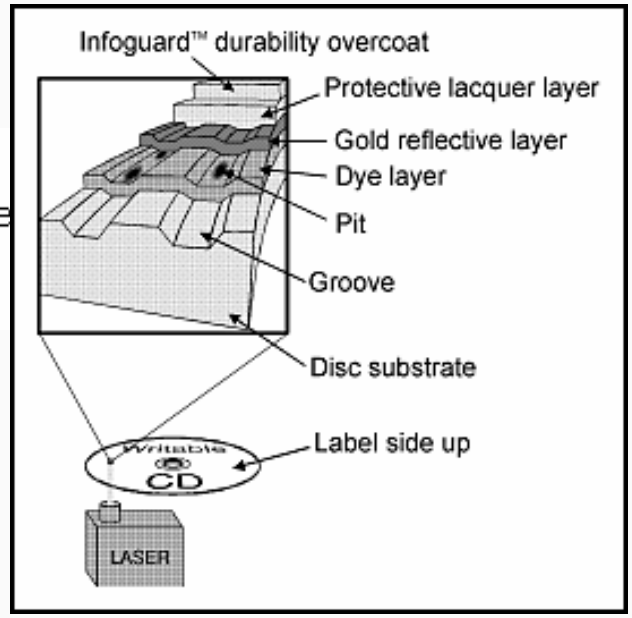


Optics involved only in reading

Optical writing in CD-WORM

The physical structure of a writable CD differs from that of a CD-ROM. A writable CD is molded from polycarbonate too, but without pits. Like a long-playing phonograph record, a writable CD has a smooth spiral groove running over most of its surface. This groove, molded into the top side of the polycarbonate substrate, serves to guide the powerful laser beam that does the writing.

When you write data to a CD-R, the writing laser (which is much more powerful than the reading laser) **heats up** the dye layer and changes its transparency. The change in the dye creates the equivalent of a non-reflective bump. This is a permanent change, and both CD and CD-R drives can read the modified dye as a bump later on.



Dye doped polymers used as the medium: light (at suitable wavelength) is heavily absorbed by the dye leading to a temperature increase and a change in optical properties

Organic dye-in-polymer (DIP) medium for write-once-read-many (WORM) optical discs

Abstract

A dye containing solution composition for use in forming optical recording media comprises about 0.1 to about 5 parts cyanine dye; about 0.1 to about 5 parts polyvinyl acetate resin and about 100 to about 90 parts co-solvents. The dye containing solution is applied to a substrate of an optical recording medium by a spin coating process to form a recording layer having a uniform thickness. The resultant optical recording medium is suitable for reading and writing with a laser beam.

Grooves are frequently scribed on the substrate to enhance optical absorption, so favoring writing

www.kodak.com

Phase changing materials I (CD-RW)

Phase change recording [1] is based upon the reversible transformation of small regions of an active layer between the crystalline and amorphous state (Figure 1). The crystalline film is heated rapidly by a focussed laser beam and melts locally. After the laser beam is turned off, the film is cooled rapidly (cooling rate > 10^9 K/s). This leads to a drastic reduction of atomic mobility which is negligible at room temperature. Hence the atoms do not return to the stable, crystalline state but are trapped in a metastable, amorphous state. Figure 2 shows the result of a structure investigation of the crystalline and amorphous state [2].

While a majority of materials can be amorphized by a short, intense laser pulse only few materials show a very pronounced difference in optical properties between the amorphous and crystalline state. This is depicted in Figure 3. Since the optical properties of the amorphous and crystalline state differ significantly (see Figure 3), different material states can be detected by a weak laser beam.

Year	Composition
1971	Te-Ge-Sb-S
1974	Te-Ge-As
1983	Te-Ge-Sn-O
1985	Te-Sn-Se, Ge-Se-Ga
1986	Te-Ge-Sn-Au, Sb_2Se, In-Se, GeTe, Bi-Se-Sb, Pd-Te-Ge-Sn
1987	GeTe-Sb_2Te_3, ($Ge_2Sb_2Te_5$, $GeSb_2Te_4$), In-Se-Tl-Co
1988	In-Sb-Te, In_3SbTe_2
1989	GeTe-Sb_2Te_3-Sb, Ge-Sb-Te-Pd, Ge-Sb-Te-Co, Sb_2Te_3-Bi_2Se_3
1991	Ag-In-Sb-Te

Table 2: History of materials development for phase change media.

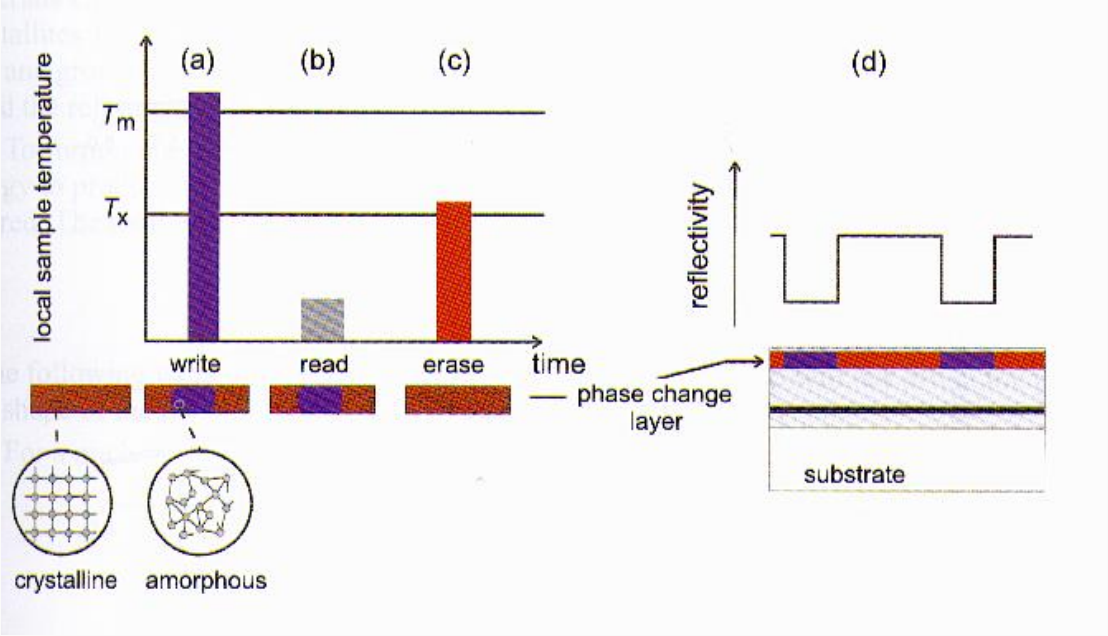


Figure 1: Principle of data storage with phase change media: To write a bit, the crystalline layer is locally molten. Recrystallization is prevented by the very high cooling rate (10^9 K/s), 'freezing' the disorder of the melt, which leads to an amorphous region. The amorphous and the crystalline areas have rather different optical properties, leading to a difference in reflectance ((b) and (d)). By a laser beam of intermediate intensity the amorphous region is heated above the glass transition temperature, so that recrystallization can take place and the bit is erased (c).

Phase changing materials II

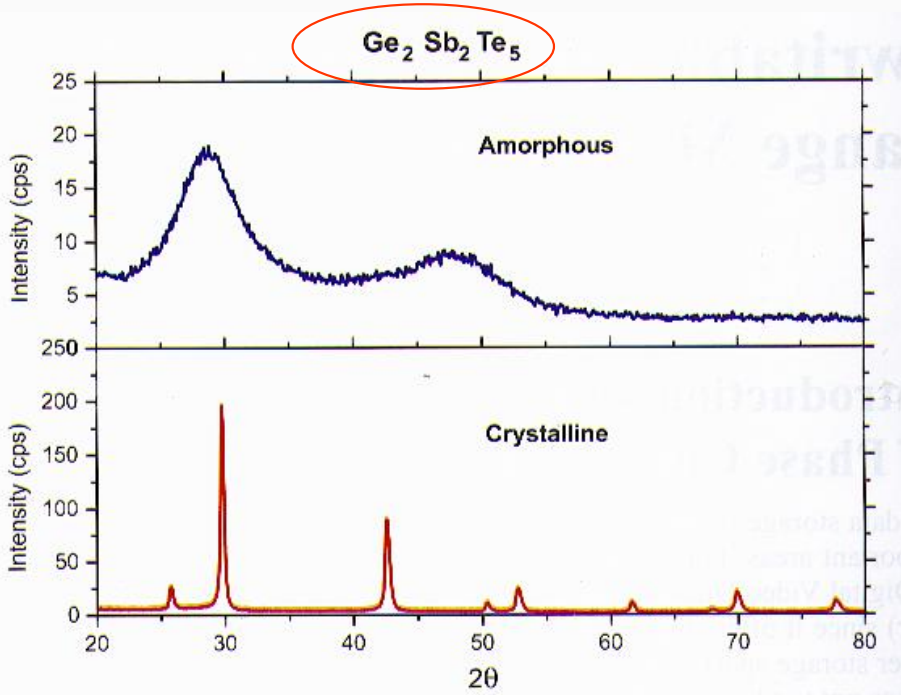
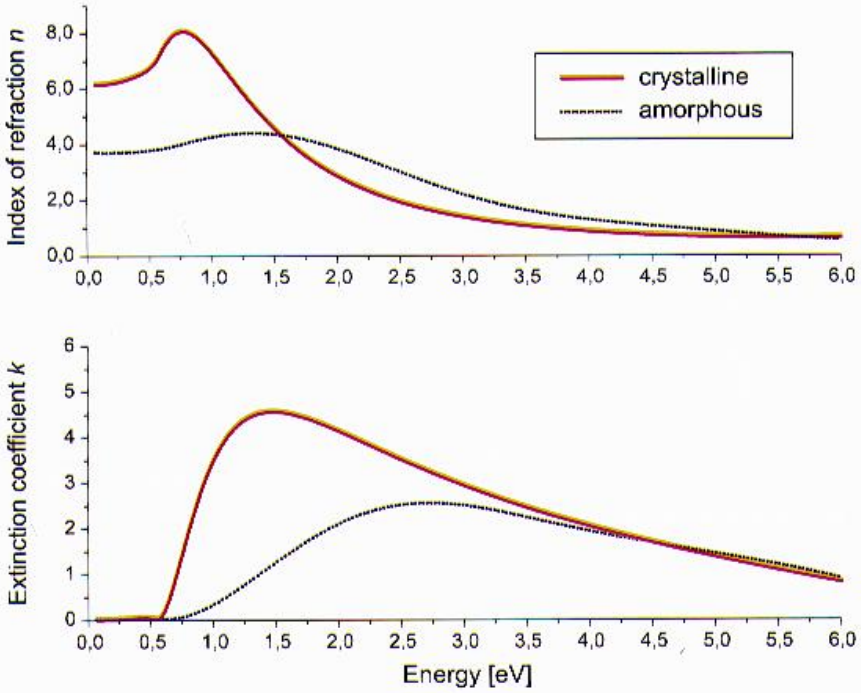


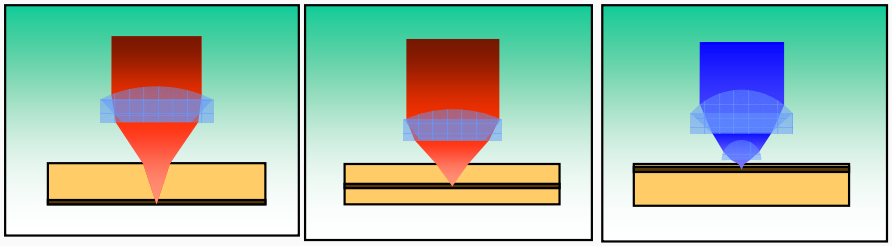
Figure 1: x-ray diffraction spectrum of a thin film of phase change material ($Ge_2Sb_2Te_5$) after deposition (amorphous) and after heating to 200°C (crystalline).

Figure 3: Index of refraction *n* and extinction coefficient *k* for amorphous (dashed line) and crystalline (solid line) $Ge_2Sb_2Te_5$.

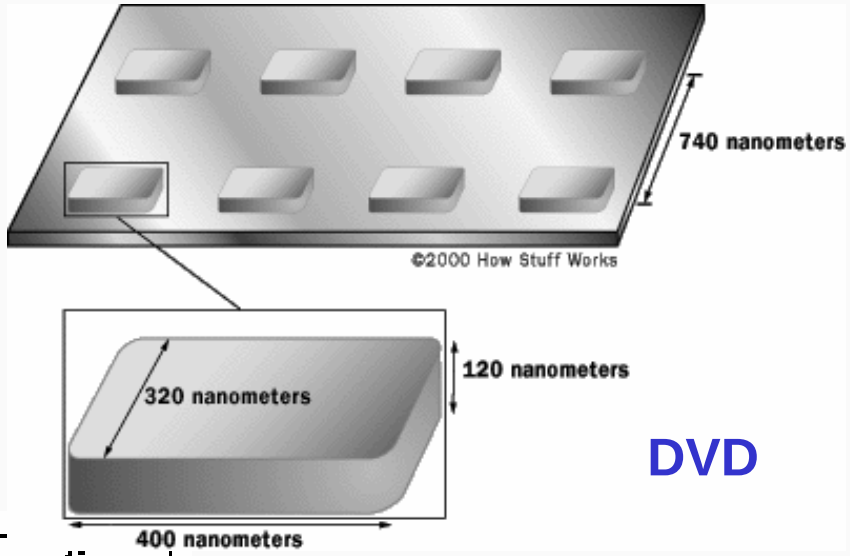


Phase changing materials exist with remarkable dependence of reflectivity on the phase (cryst/amorph)

Fundamental limits in optical systems



	CD	DVD	DVR
λ (nm)	780	650	400
NA	0.45	0.6	0.85
Capacity (GB)	0.65	4.7	22



Parameter	CD	DVD	4th Generation
λ (nm)	780	650	400
NA	0.45	0.60	0.85-1.5
Track pitch (μm)	1.6	0.74	0.3-0.15
Velocity (m s-1)	1.2	4.0	3-25
Substrate thickness (mm)	1.2	0.6	1.2-2
Spot size λ/2NA (μm)	0.9	0.55	0.25-0.13
Capacity (GB)	0.65	4.7	100

Laser spot minimum size is affected by diffraction (we will see more!)

⇩

Optics with larger NA and lasers with shorter wavelength must be used to increase the storage density

Technological limits in optical systems

A.C. Ferrari,
Cambridge University

At present, diode lasers are not available with $\lambda < 400$ nm (material/device problem, we will see, perspectives are to reach ~ 350 nm)

Writing laser intensity must be large enough, and topographical modifications of the written layer cannot be ruled out (but they should be)

Greater NA means shorter focal lengths

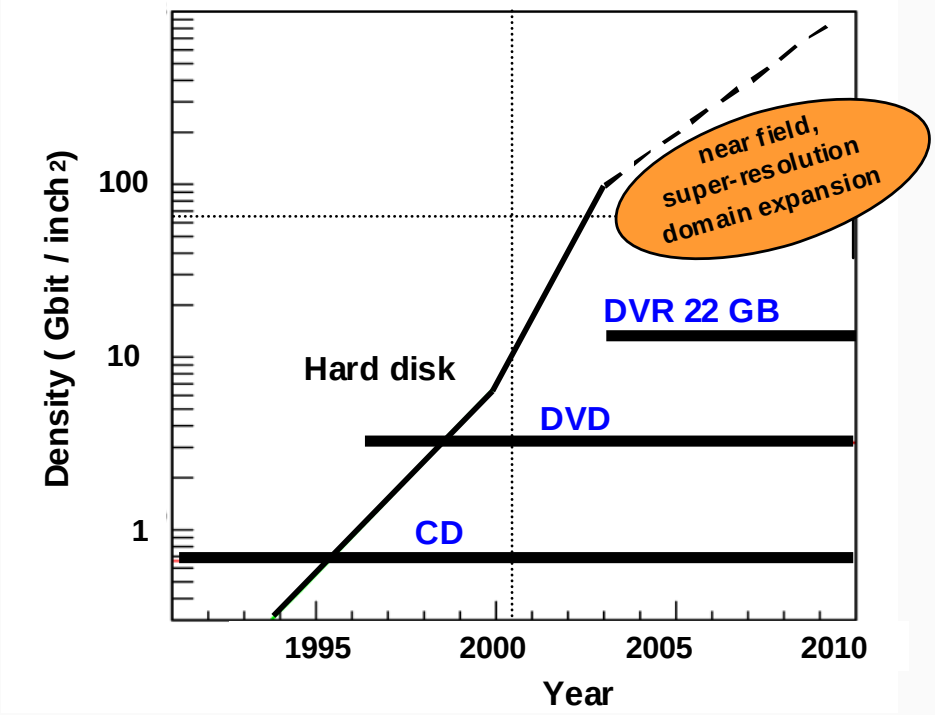
⇩

The objective is practically in contact with disk

Layers for optical coatings must be defect-free on a sub-micron scale

⇩

Deposition techniques (usually, spin-coating) must be improved



Technological limitations may be (partially) solved, but only alternative approaches hold the possibility to overcome any limit

⇩

Optical near field??
(we will see more on the tech.)

Photopolymers I

5 Photoaddressable Polymers

5.1 Introduction

Polymers are perfect materials for a diversity of applications. Due to their macromolecular architecture there is an enormous variety to modify and control the synthesis of polymers. Thus, they can be tailored to even quite difficult demands. Since a whole industry deals with the processing of polymers, efficient production lines have been developed for almost every polymer. Not only the molecular composition, but also the cost of polymers has been optimized. Now these materials can be considered even for highly sophisticated applications, as optical and holographic data storage.

Looking at the development of optical media, it is obvious that polymeric materials play a major role for the compact disc (CD): Important for the success of the CD-ROM and CD-AUDIO was the development of a specific polymer – polycarbonate – which serves as substrate material, carrying the digital information in the form of tiny pits. In the ROM the information is imprinted during production and cannot be erased.

In photopolymers the optical information is stored by changing the optical properties of the material by a light-induced polymerization or a ring opening reaction. These materials turned out to be the most suitable holographic media for write-once-read-many (WORM) applications [66]. Since especially the optical requirements for holographic data storage are very stringent, there are some drawbacks that hinder the introduction of those polymers into mass production. So far, the shrinkage during illumination is the most severe problem for photopolymers.

As far as rewritable holographic storage is concerned, photorefractive crystals like iron-doped lithium niobate ($LiNbO_3$) are mostly used for rewritable (R/W) laboratory demonstrations [67]. In the following chapter, a polymeric class of materials, the so-called photoaddressable polymers [68] - [72] and the results of holographic measurements with these materials will be presented. These polymers show no shrinkage effects and react in a reversible way to the illumination of light and are therefore able to meet the requirements for R/W holographic data storage.

In principle, all materials that react to light with a change of specific properties can be described as photoaddressable polymers. Since the change of material properties is the basic condition for storing information in a material, we have to deal with a reversible modification in order to fulfill the requirements of an R/W material. In the following section the name photoaddressable polymer (PAP) is used as a synonym for a class of polymers with azo dyes as reversible antennae for the incident light. Those PAPs are basically azobenzene-containing side-group polymers. The aim of this chapter is to give an overview of the optical and photophysical properties of those polymers.

Purely optical modifications are accessible (without any morphology change?)

⇩

Holographic storage (and near field)

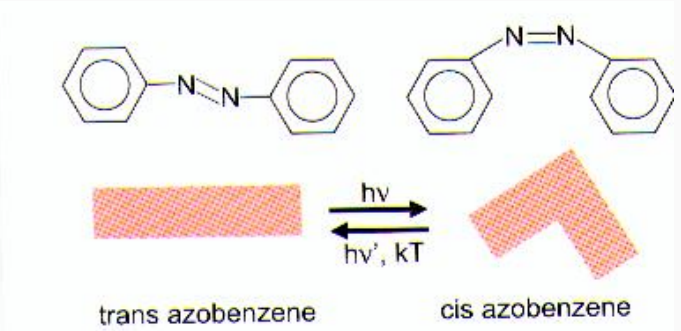


Figure 21: Trans-cis isomerization of azoben-

5.2 Photochemistry of Azobenzene

The photophysical reactions of azobenzene have been well studied. It can be demonstrated that due to controlled light-induced reactions of azo chromophores, properties of the whole system incorporating the dye can be modified. Those properties include for example viscosity, solubility, mechanical parameters, bioactivity, and optical constants [73]. Additionally azobenzene molecules can be used as a probe for their molecular surroundings. In this way a detailed study of polymeric parameters can be performed by monitoring the photochemical behavior of the azo dyes. The success of azo dyes in all these applications can be explained by detailed knowledge of their light-induced photoreactions: Azobenzene chromophores exist in two isomeric states. The rodlike long shaped trans form and the bent cis configuration. The isomerization can be induced by light in both directions, from trans to cis and from cis to trans, whereas the cis-isomer can also undergo a thermal back relaxation to the thermodynamically more stable trans-isomer (Figure 21).

A look at a typical absorption spectrum (Figure 22) of unsubstituted azo chromophores (Figure 21) shows two absorption bands: The so-called $\pi\pi^*$ band with a maximum absorbance at $\lambda_{max} \sim 360$ nm and the so-called $n\pi^*$ band with $\lambda_{max} \sim 460$ nm. The spectral position of the absorption maximum of the $\pi\pi^*$ band can be shifted by chemical modification of the dye, namely by the replacement of donor/acceptor substituents. Those substituents do not influence the spectral position of the $n\pi^*$ band. The isomerization cycles have a distinct influence on absorption and optical index, which can be used for data recording.

The absorption bands define the laser wavelength needed: Azo-dyes undergo their isomerization cycles by illumination with light of wavelengths from the UV to the green/yellow range of the optical spectrum.

Photopolymers II

5.3 Azobenzene-Containing Polymers

There are three ways to incorporate chromophores into a polymer:

- In guest-host-systems chromophore guests are doped into a polymeric host. In these systems the chromophore concentration cannot exceed a specific value, because highly concentrated chromophores tend to phase separation and crystallization.
- This disadvantage can be avoided by attaching the chromophores to the backbone as side chains.
- Or the chromophores are fixed as part of the main chain.

The first investigations of the isomerization kinetics of azo chromophores in polymers were performed in 1972 [74] and mainly focused on spectroscopic measurements [75] – [78]. Those experiments can be summarized by the experimental observation that the isomerization of azo dyes in a polymeric environment is possible, even at temperatures below the glass transition temperature. This result applies to side chain as well as to main chain polymers.

Since the isomerization results in a change of the molecular shape of the azo chromophores, as described above, there is a specific demand for free volume to enable this reaction[4]. In solution this free volume condition is fulfilled. In polymers, however, there might be some sterical constraints due to the inhomogeneous free volume distribution. For some chromophores there are local environments with large free volume, where the isomerization can be performed in a similar way as in solution. But there are also configurations where the free volume is not sufficient for the isomerization of the dyes. Therefore strong deviations of the photochemical reactions in polymers occur, if compared to the reactions in a solution.

However, experiments performed in polymeric systems demonstrate that azo dyes are able to undergo isomerization reactions in this environment.

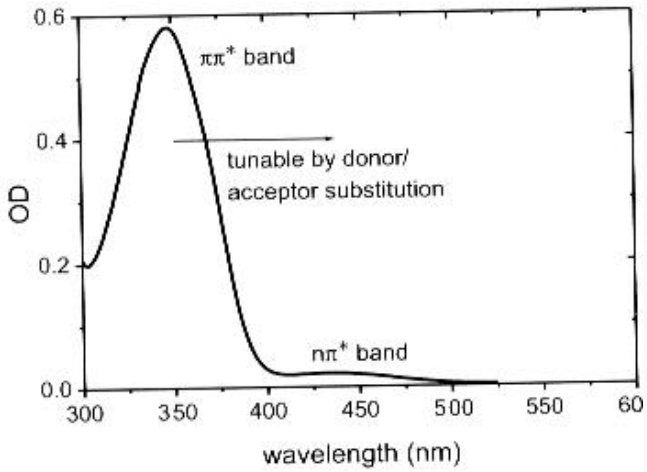
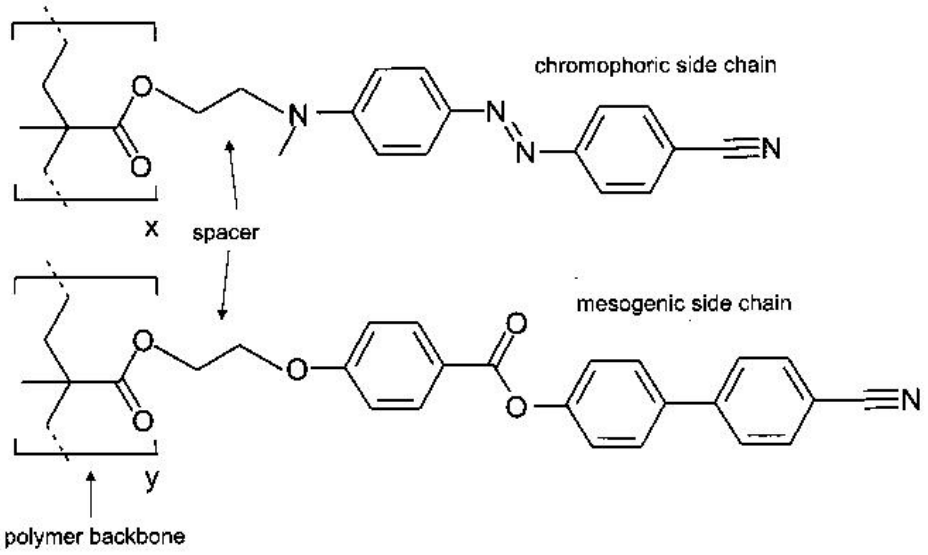


Figure 22: Absorption spectrum of unsubstituted azobenzene in solution.

5.5 Photoaddressable Polymers for Optical Storage

The motivation of the development of polymers following the scheme of Figure 23 can be summarized as follows:

- The dye acts as an antenna for the incident light. In order to optimize the response to light, adequate dye systems must be used. Azo dyes are the perfect chromophores for this purpose because of their well-known photochemistry.
- It is the task of the mesogenic groups to stabilize and to amplify the reorientation of the chromophores. The physical reason for this can be explained by the intrinsic tendency of the mesogens to spontaneously organize in domains.



Photopolymers can be engineered to improve their properties (e.g., to limit the topography changes upon irradiation)

Photopolymers and near-field (an introduction)

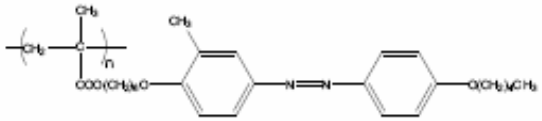


Figure 4.2: Schematic of the azo-polymer we used for near-field lithography (*PMA*4). *PMA*4 is polymethacrylate (*PMA*) containing 3-methyl-4′-pentyloxy-azobenzene unit connected at the 4-position of the main polymer chain via six hexamethylene spacers.

Near-field illumination has already been used for pure optical lithography on *PMA*4 samples [132]. This technique has provided (see also next section) sub-wavelength resolution. The best resolution achieved in this process until now is of 120 nm [132]. The application of near-field microscopy (SNOM) in pure-optical lithography on azo-based polymers leads to estimated potential storage density of at least 1 Gbit/cm^2.

Material engineering

the spacer length is adjusted to obtain both stability of the azo-molecules configurations in the polymer and a liquid crystaline phase, particularly appreciated for holographic high density data storage (see next section). As a result, the glass transition temperature of the resulting compounds ranges into the interval 30°C-100°C.

The rate of thermal isomerization from *cis* to *trans* configuration is negligible with respect to the rate of photo-activated transitions. In order to achieve light-driven complete *trans-cis-trans* isomerization cycles, research is oriented towards materials presenting *trans-to-cis* absorption band superimpose to *cis-to-trans* absorption band. Following the classification introduced by Rau [117], these materials are the so called *pseudostilbenes*, i.e., azobenzene-based polymers containing electron-donor and electron-acceptor substituents connected to the azobenzene groups. *Pseudostilbenes* have a $\pi-\pi^\star$ band practically superimposed to $n-\pi^\star$ band allowing light-induced excitation from *trans-to-cis* and *cis-to-trans* using the same light source.

Photopolymers can be envisioned as suitable materials for near-field optical writing (we will see more!)

Write mechanism

Since the pioneering work by Todorov et al. [121], azobenzene containing polymers have been largely studied as materials for high density data storage. Due to the rod-like shape of the azobenzene *trans* isomer, in the light driven isomerization, the transition momentum of *trans-cis* isomerization has its maximum when the molecule is oriented along the light polarization direction. Thus, complete *trans-cis-trans* isomerization cycles driven by illumination with linearly polarized light yields to a statistical orientation of the azo-moieties perpendicularly to the light polarization direction.

The orientation of azo-moieties perpendicularly to the light polarization direction results into the variation of the refractive index components inside the polymeric compound as has been studied using attenuated total reflection (ATR) [42]. As a consequence, a modification of the properties of azo-containing polymers occurs under illumination. This phenomenon has suggested azo-based polymers as material for holographic data stor-

Birefringence patterns are written well below the glass transition temperature of the polymeric compound and are stable for months. Nevertheless the written data may be erased by heating the sample above its glass transition temperature (T_g) or by exposure to a single circularly polarized light beam that destroys the order among the azo-molecules [125]. The writing process is not energetically

Antonio Ambrosio, PhD Thesis Appl. Phys., Pisa 2005 (unpublished)

A nanotechnological perforated card: the "millipede"

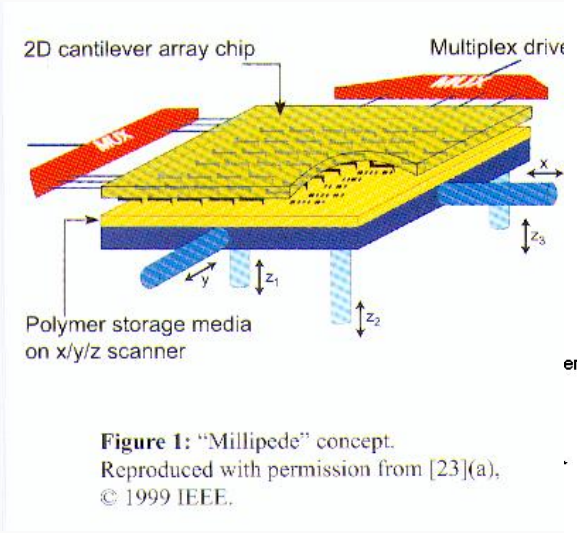


Figure 1: "Millipede" concept.
Reproduced with permission from [23](a), © 1999 IEEE.

2 The Millipede Concept

The 2D AFM cantilever array storage technique [9], [10] called "Millipede" is illustrated in Figure 1. It is based on a mechanical parallel *x/y* scanning of either the entire cantilever array chip or the storage medium. In addition, a feedback-controlled *z*-approaching and -leveling scheme brings the entire cantilever array chip into contact with the storage medium. This tip-medium contact is maintained and controlled while *x/y* scanning is performed for write/read. It is important to note that the Millipede approach is not based on individual *z*-feedback for each cantilever; rather, it uses a feedback control for the entire chip, which greatly simplifies the system. However, this requires stringent control and uniformity of tip height and cantilever bending. Chip approach and leveling make use of four integrated approaching cantilever sensors in the corners of the array chip to control the approach of the chip to the storage medium. Signals from three sensors (the fourth being a spare) provide feedback signals to adjust three magnetic *z*-actuators until the three approaching sensors are in contact with the medium. The three sensors with the individual feedback loop maintain the chip leveled and in contact with the surface while *x/y* scanning is performed for write/read operations. The system is thus leveled in a manner similar to an antivibration air table. This basic concept of the entire chip approach/leveling has been tested and demonstrated for the first time by parallel imaging with a 5 × 5 array chip [11]. These parallel imaging results have shown that all 25 cantilever tips have approached the substrate within less than 1 μm of *z*-actuation. This promising result has led us to believe that chips with a tip-apex height control of less than 500 nm are feasible. This stringent requirement for tip-apex uniformity over the entire chip is a consequence of the uniform force needed to minimize or eliminate tip and medium wear due to large force variations resulting from large tip-height nonuniformities [4].

AFM-tip

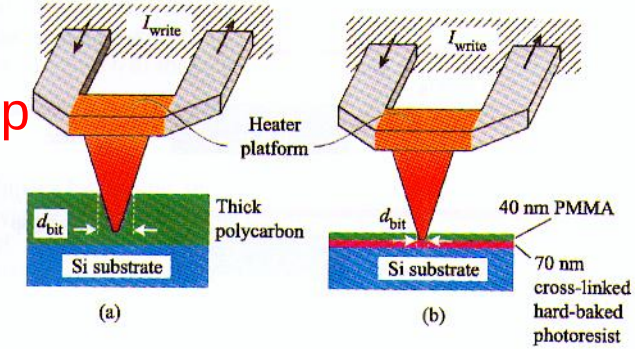
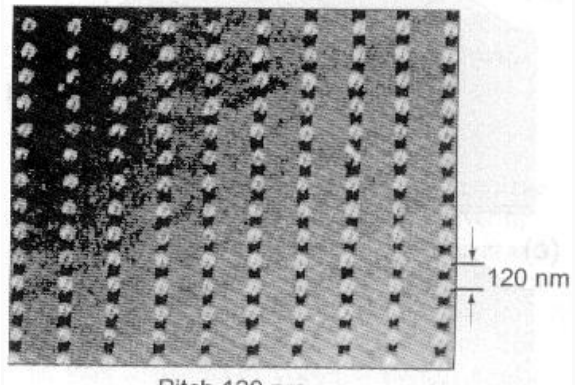


Figure 2:
(a) Earlier storage medium consisting of a bulk polycarbonate layer.
(b) New storage medium for smaller bit sizes, consisting of a thin writable PMMA layer on top of Si substrate separated by a cross-linked film of photoresist.
From [13], reproduced with permission.



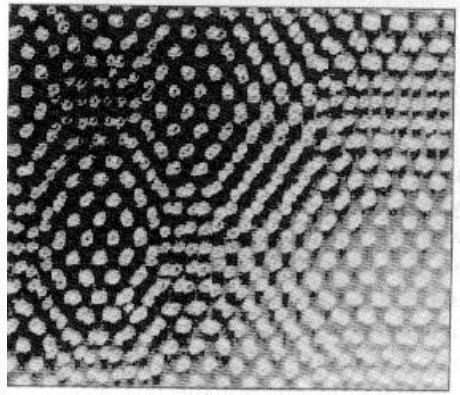


Figure 3: Series of 40-nm data bits formed
n an uniform array with
a) 120-nm pitch and
b) variable pitch (≥ 40 nm), resulting in bit
real densities of up to 400 Gb/inch^2.
mages obtained with a thermal readback
echnique.
Adapted from [13], with permission.

Nanotechnology can be proposed to use old and traditional methods in a new, advanced context

Conclusions

✓ Miniaturization in data storage is a key point for increasing performance in Information Technology

✓ A variety of methods, materials, techniques exist for data storage

✓ Steps towards nanosized data storage must face fundamental, technical, material problems

✓ Nanotechnology can provide data storage with new and more powerful methods (but still to be fully developed)